ANALOG ELECTRONICS

AIM & OBJECTIVES:

- To acquaint the students with construction, theory and characteristics of P-N junction diode
- Analyze the different application of diodes
- To familiarize the student with the analysis and modelling of diode.
- Understand the characteristics of transistors.
- Design and analyze various rectifier and amplifier circuits. Design sinusoidal and non-sinusoidal oscillators.
- Understand the functioning of OP-AMP and design OP-AMP based circuits.

PRE TEST

1. What is the barrier potential of a Silicon diode and Germanium Diode at room temperature?

   a) Si=0.3, Ge=0.7
   b) Si=0.7, Ge=1
   c) Si=1, Ge=0.3
   d) Si=0.7, Ge=0.3

2. Which is the most widely used semiconductor?

   a) Copper
   b) Germanium
   c) Silicon
   d) None of the above

3. The depletion region or space charge region or transition region in a semiconductor p-n junction diode has

   a) Electrons and holes.
   b) Positive ions and electrons.
   c) Positive and negative ions.
   d) Negative ions and holes

4. In a P-N junction the positive voltage at which the diode starts to conduct consequently is called.

   a) Cut off voltage
   b) Saturation voltage
   c) Knee voltage
   d) Breakdown voltage

5. A diode

a) Is the simplest of the semiconductor devices
b) Has a characteristic that closely follows that of a switch
c) Is two terminal device
d) All of the mentioned

6. The emitter current I_E in a transistor is 3mA. If the leakage current I_{CBO} is 5µA and α=0.98, calculate the collector and base current.
a) 3.64mA and 35µA
b) 2.945mA and 55µA
c) 3.64mA and 33µA
d) 5.89mA and 65µA

7. In CB configuration, the value of α=0.98A. A voltage drop of 4.9V is obtained across the resistor of 5KΩ when connected in collector circuit. Find the base current.
a) 0.01mA
b) 0.07mA
c) 0.02mA
d) 0.05mA

8. For a MOSFET Vgs=3V, Idss=5A, and Id=2A. Find the pinch of voltage Vp
a) 4.08
b) 8.16
c) 16.32
d) 0V

9. The approximate input impedance of the opamp circuit which has Ri = 10k, Rf = 100k, RL = 10k

a)∞

b) 120k

c)110k

d) 10k

10. Calculate the frequency of oscillation for RC phase shift oscillator having the value of R and C as 5Ω and 7µF respectively.
a) 1230 Hz
b) 1857 Hz
c) 502Hz
d) 673 Hz

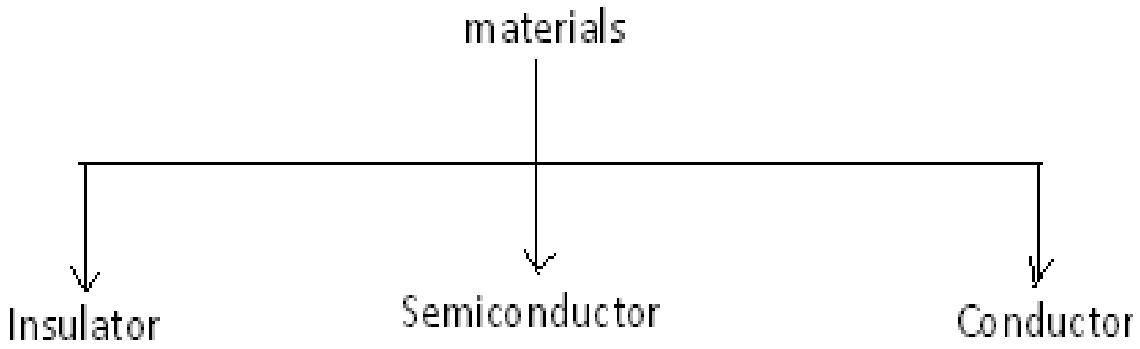
PREREQUISITE :

- Knowledge about PN junction, biasing
- Should know about circuit analysis.

MODULE I - DIODE CIRCUITS

INTRODUCTION

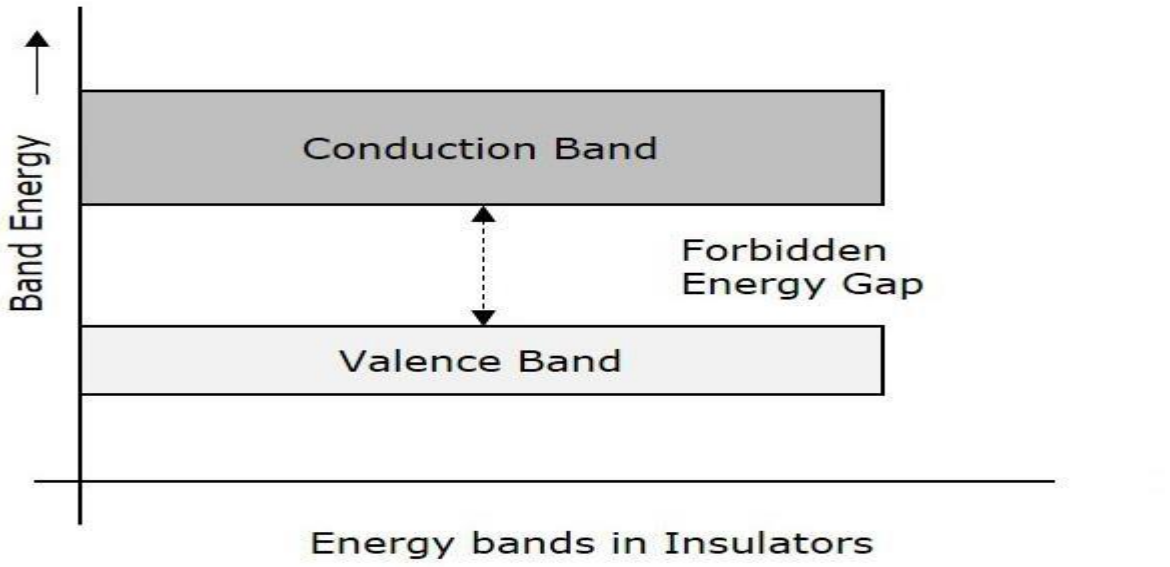
Based on the electrical conductivity all the materials in nature are classified as insulators, Semiconductors, and conductors



INSULATOR

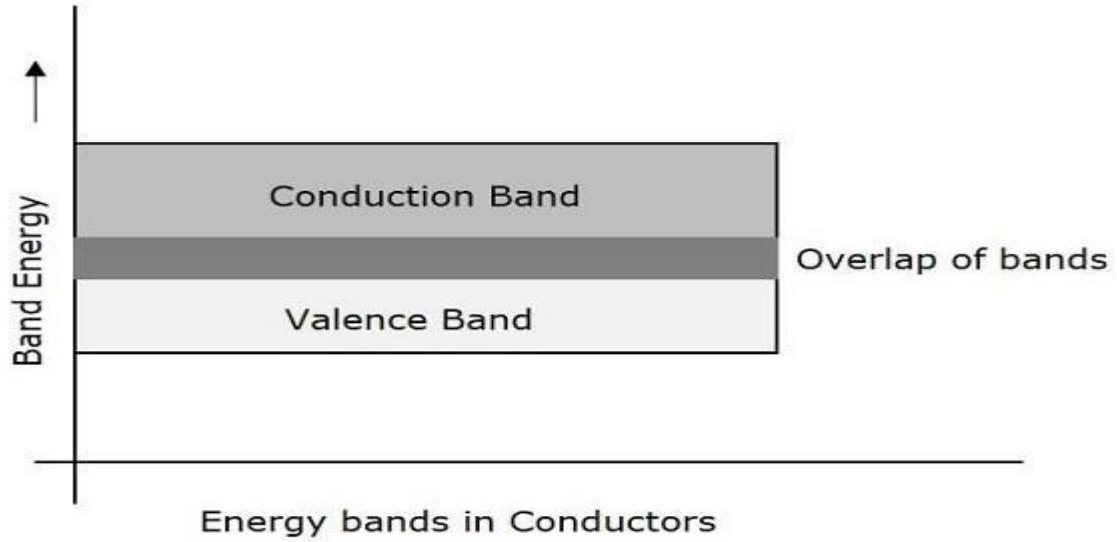
An insulatorisamaterialthatoffersaverylow level (or negligible) of conductivity when voltage is applied.

- Eg: Paper,Mica,glass,quartz.
- Typical resistivity level of an insulator is of the order of 1010 to 1012 Ω-cm.



CONDUCTOR

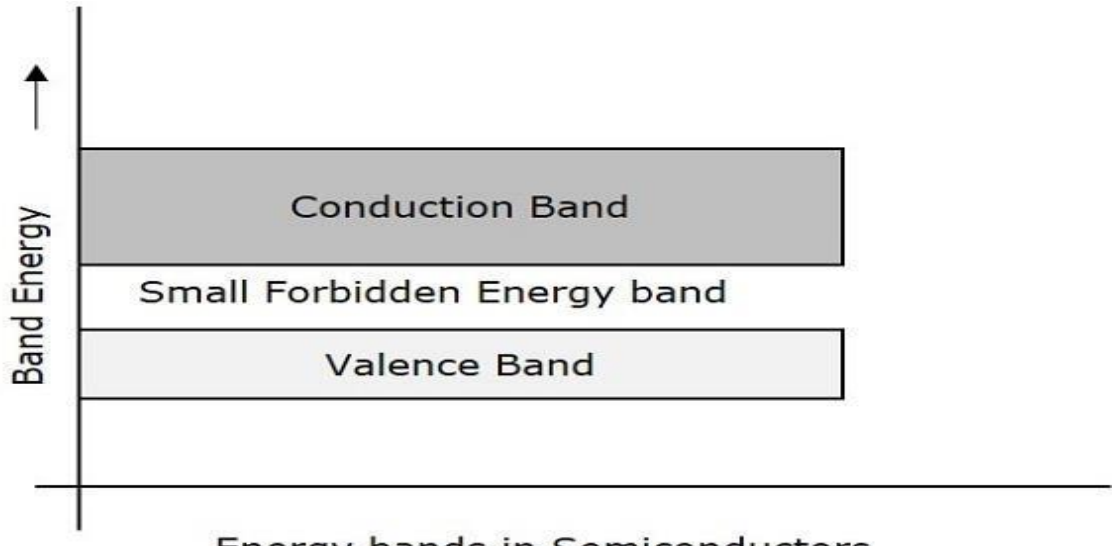
- A conductor isamaterialwhichsupportsa generousflow of chargewhenavoltageis applied across terminals.i.e.it hasvery high conductivity.
- Eg:Copper,Aluminum,Silver, Gold.
- Theresistivityofaconductorisintheorderof 10^{-4} and $10^{-6}\Omega$-cm.



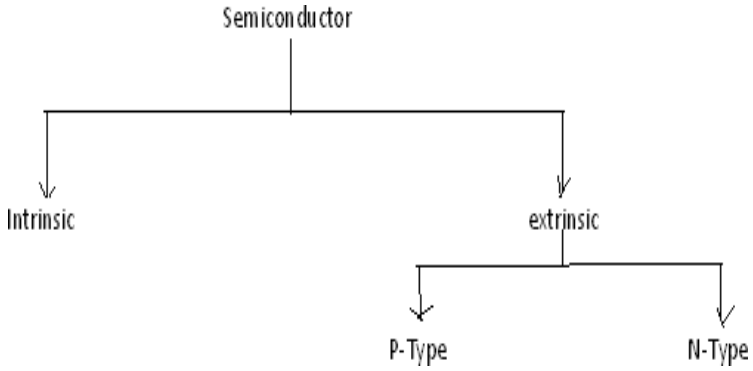
Energy bands in Conductors

SEMICONDUCTOR

- A semiconductor is a material that has its conductivity somewhere between the insulator and conductor.
- The resistivity level is in the range of 10and104 Ω-cm.
- Two of the most commonly used are Silicon (Si=14 atomic no.) and germanium (Ge=32 atomic no.).



Energy bands in Semiconductors



INTRINSIC SEMICONDUCTOR

- Apureformofsemiconductorsiscalledas intrinsic semiconductor. Conduction in intrinsic semiconductor is either due to thermalexcitationorcrystaldefects.
- Si and Ge are the two most important semiconductors used.Other examples include Gallium arsenide GaAs, Indium Antimonide (InSb) etc.

EXTRINSIC SEMICONDUCTOR

- Intrinsic semiconductor hasverylimitedapplicationsas theyconductverysmallamounts ofcurrentatroom temperature.
- The current conduction capability of intrinsic semiconductorcanbeincreased significantlybyadding a small amounts impurity to the intrinsic semiconductor.
- By adding impurities it becomes impure or extrinsic semiconductor.This process of adding impuritiesis called as doping.
- The amountof impurity added is1part in10^6atoms.

N-TYPE SEMICONDUCTOR

- If the added impurity is a pentavalent atom thentheresultantsemiconductoriscalled N- typesemiconductor.
- Examples of pentavalent impurities are Phosphorus, Arsenic, Bismuth, Antimony etc

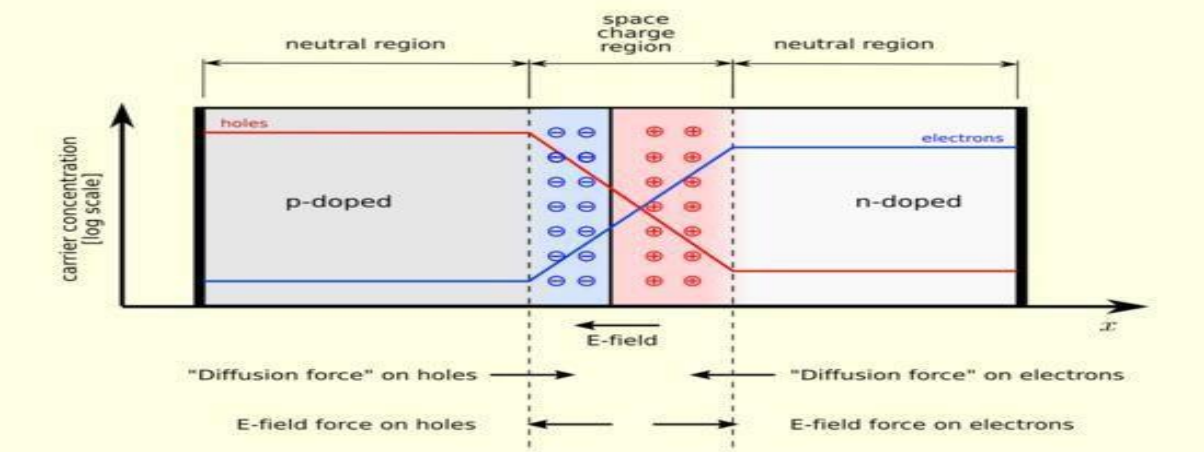
P-TYPE SEMICONDUCTOR

- If the added impurity is a trivalent atom then the resultant semiconductor is called P-type semiconductor.
- Examplesof trivalent impuritiesareBoron, Gallium , indiumetc.

PN JUNCTION

- In a piece of semiconductor, if one half is dopedby ptypeimpurityand theother halfis doped by n type impurity, a PN junction is formed.
- The plane dividing the twohalves or zones is called PNjunction.

- At the junction thereisa tendency of free electrons to diffuse over tothePside and theholes tothe N side. Thisprocessiscalleddiffusion.
- As the free electrons move across the junction from N type to P type, the donor atoms become positively charged.
- Hence a positive chargeisbuilton the N-side ofthe junction.Thefreeelectronsthatcrossthe junction uncover the negative acceptor ions by filing the holes. Therefore a negative charge is developedonthep– side of thejunction.



- This net negative charge on the p side preventsfurtherdiffusionofelectronsintothe p side.
- SimilarlythenetpositivechargeontheNside repelstheholecrossingfrompsidetoNside.
- Thusabarriersissetupnearthejunction whichpreventsthefurthermovement of chargecarriersi.e. electronsandholes.
- An electrostatic potential difference is established between P and N regions, which are called the potential barrier, junction barrier, diffusion potential or contact potential, Vo.
- The magnitude of the contact potential Vo varieswithdopinglevelsandtemperature. Vo is0.3V for Geand0.72VforSi.
- Thejunctionregionisdepletedofmobile charge carriers.Henceitiscalleddepletionlayer,space region, and transitionregion.
- The depletion region is of the order of 0.5μm thick.Therearenomobilecarriersinthisnarrow depletion region.
- Hencenocurrentflowsacrossthejunctionand thesystemisinequilibrium.
- Tothe left of this depletion layer, the carrier concentrationisp=NAandtoitsrightitisn=ND.

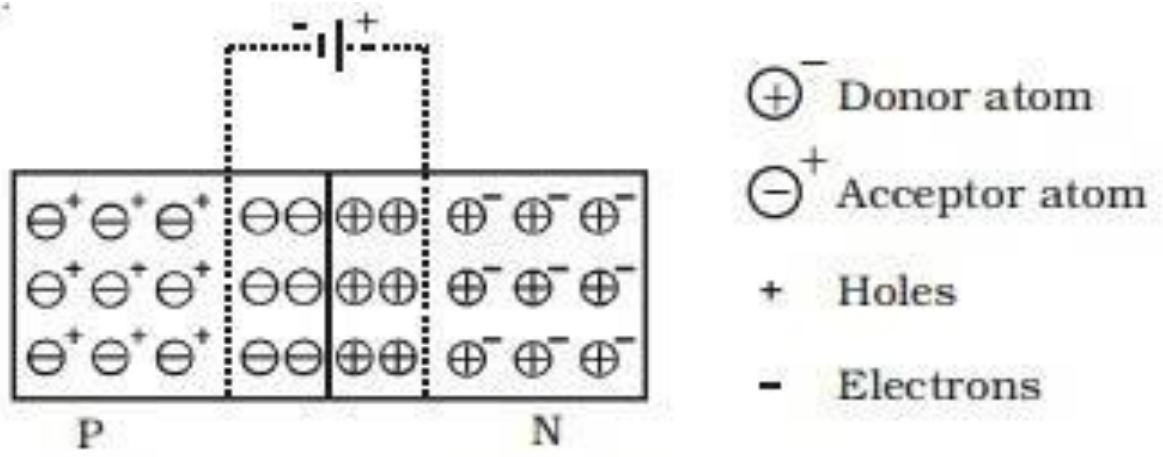


Fig P N Junction diode

FORWARD BIASED JUNTION

- When a diode is connected in a Forward Bias condition, a negative voltage is applied to the Ntype materialandapositivevoltageisapplied to the P-typematerial.
- If this external voltage becomes greaterthanthe valueofthepotentialbarrier,approx.0.7voltsfor silicon and 0.3 volts for germanium, the potential barriers opposition will be overcome and current will start to flow.
- This is because the negative voltagepushesorrepelselectronstowardsthe junction giving them the energy to cross over and combine with the holes being pushed in the opposite direction towards the junction by the positive voltage.

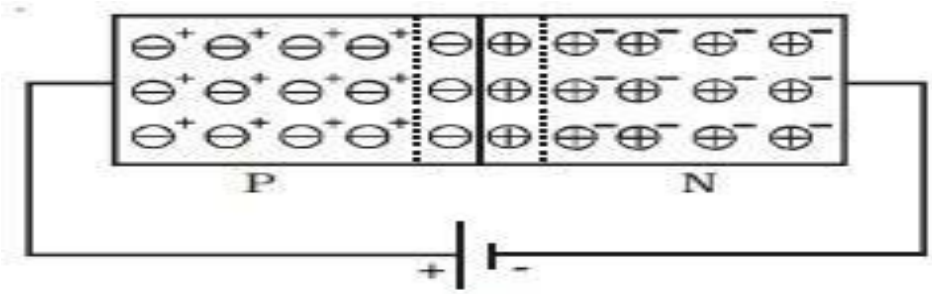
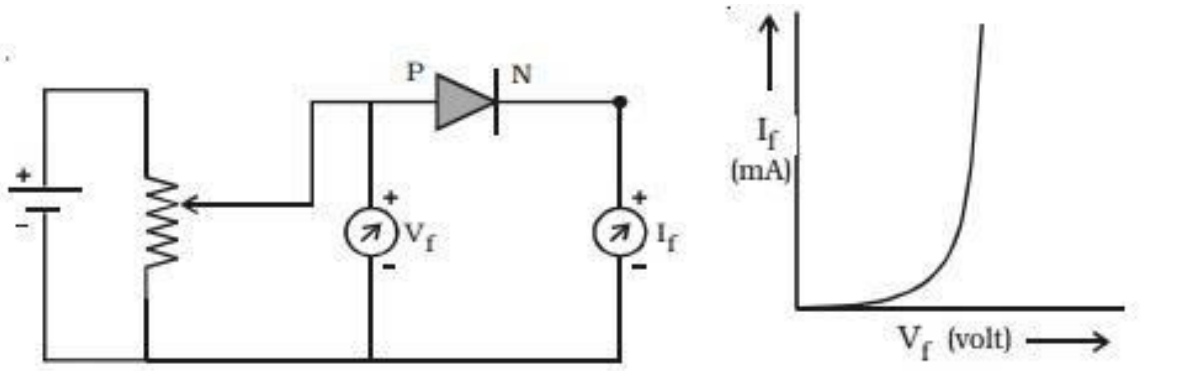


Fig Forward biased PN junction diode



(a) Diode circuit–Forward bias *(b) Forward characteristics*

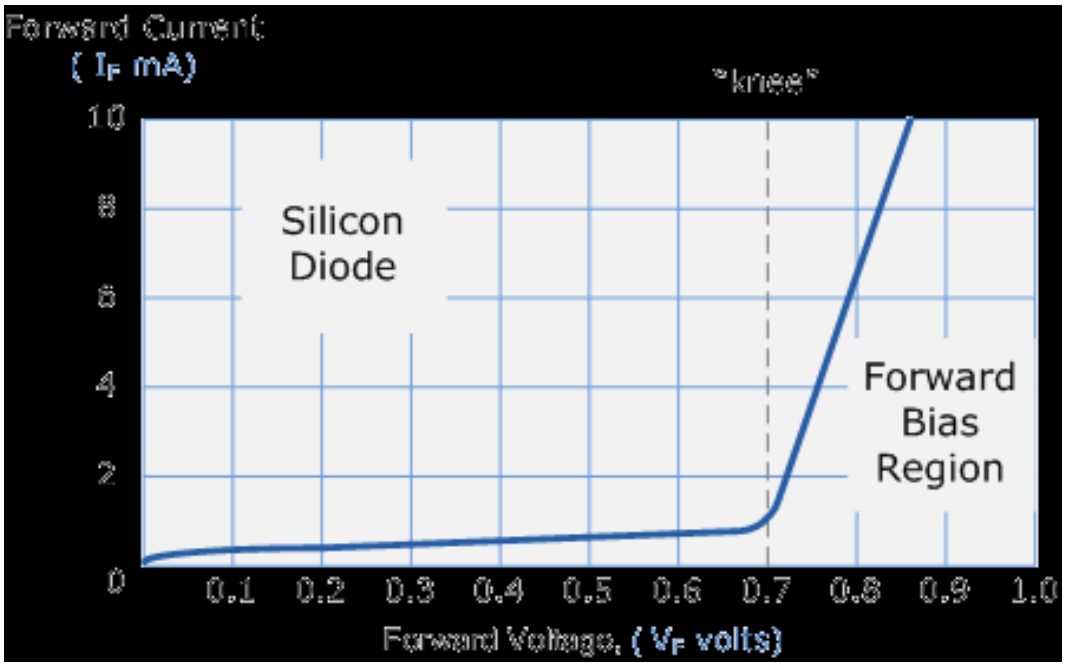
Fig Forward bias characteristics of a diode

Forward Characteristics Curve for a Junction Diode

This results in a characteristics curve of zero current flowing up to this voltage point, called the "knee" on the static curves and then a high current flow through the diode with little increase in the external voltage.

FORWARD BIASED JUNCTION DIODE

- The application of a forward biasing voltage on the junction diode results in the depletion layer becoming very thin and narrow which represents a low impedance path through the junction thereby allowing high currents to flow.
- The point at which this sudden increase in current takes place is represented on the static I-V characteristics curve above as the "knee" point.



REVERSEBIASED JUNCTION

- When a diode is connected in a Reverse Bias condition, a positive voltage is applied to the N-type material and a negative voltage is applied to the P-type material.
- The positive voltage applied to the N-type material attracts electrons towards the positive electrode and away from the junction, while the holes in the P-type end are also attracted away from the junction towards the negative electrode.
- The net result is that the depletion layer grows wider due to a lack of electrons and holes and presents a high impedance path, almost an insulator. The result is that a high potential barrier is created thus preventing current from flowing through the semiconductor material.

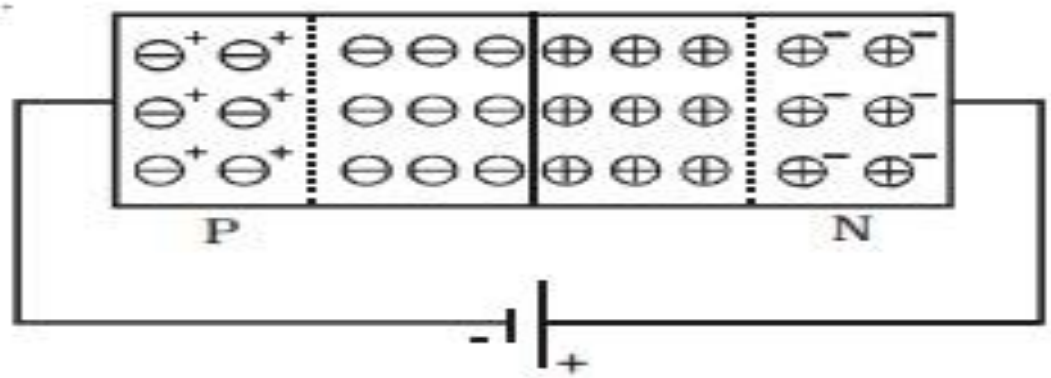
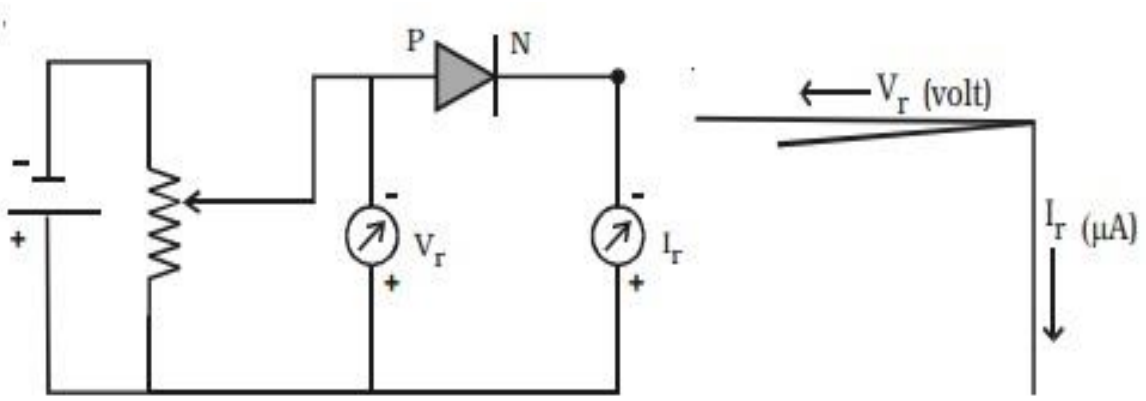


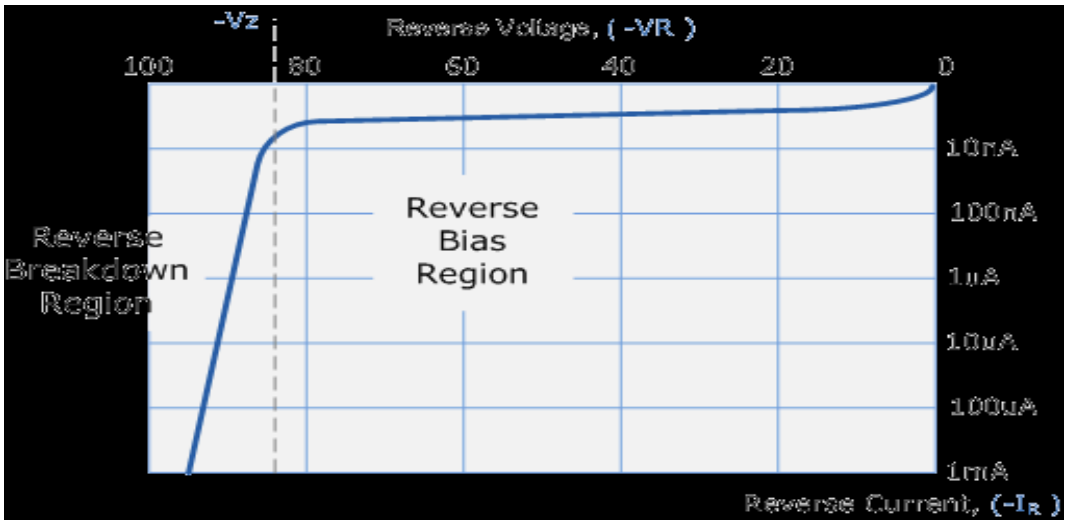
Fig Reverse biased PN junction diode.

- This condition represents a high resistance value to the PN junction and practically zero current flows through the junction diode with an increase in bias voltage. However, a very small **leakage current** does flow through the junction which can be measured in microamperes, (μA).
- One final point, if the reverse bias voltage Vr applied to the diode is increased to a sufficiently high enough value, it will cause the PN junction to overheat and fail due to the avalanche effect around the junction. This may cause the diode to become shorted and will result in the flow of maximum circuit current, and this shown as a step downward slope in the reverse static characteristics curve.



(a) Diode circuit–Reverse bias (b) Reverse characteristics

Fig Reverse bias characteristics of a diode

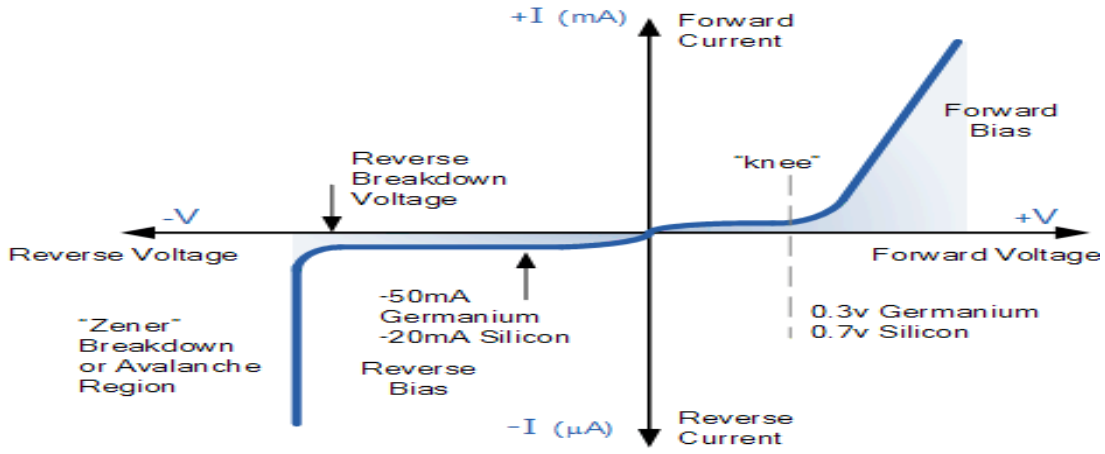


DIODE CURRENT EQUATION

$$I = I_0 \, e^{\frac{qV}{\eta KT}}$$

Where
I – Diode Current
Io- Diode reverse saturation current at room temperature
V- External Voltage applied to the diode
η – A constant, 2- Silicon and 1- Germanium
k – Boltzmann's constant, 1.38066×10^{-23}J/K
q- charge of an electron, 1.60219×10^{-19}C
T- temperature of the diode junction

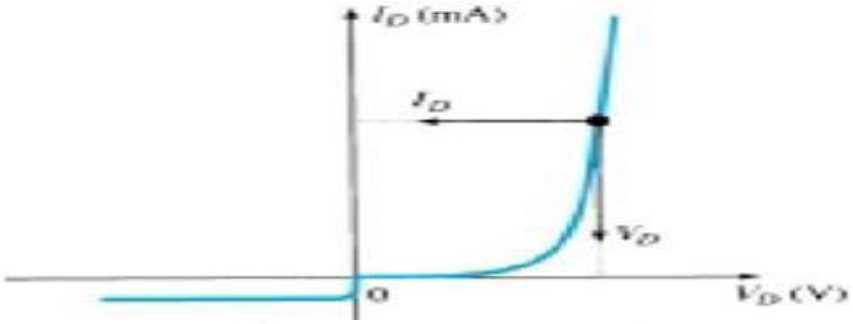
V-I CHARACTERISTICS



RESISTANCE LEVELS:

DC or Static Resistance:

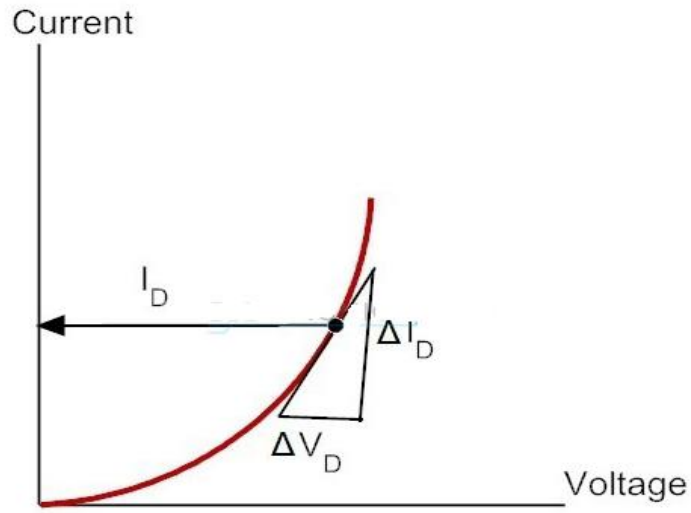
The application of a dc voltage to a circuit containing a semiconductor diode will result in an operating point on the characteristic curve that will not change with time. The resistance of the diode at the operating point can be found simply by finding the corresponding levels of VD and ID.



$$R_D = \frac{V_D}{I_D}$$

AC or DYNAMIC RESISTANCE:

- If a sinusoidal input is applied, the situation will change completely. The varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage.
- A straight-line drawn tangent to the curve through the Q-point will define a particular change in voltage and current that can be used to determine the ac or dynamic resistance.



$$r_d = \frac{\Delta V_d}{\Delta I_d}$$

BREAK DOWN MECHANISMS:

Avalanche breakdown

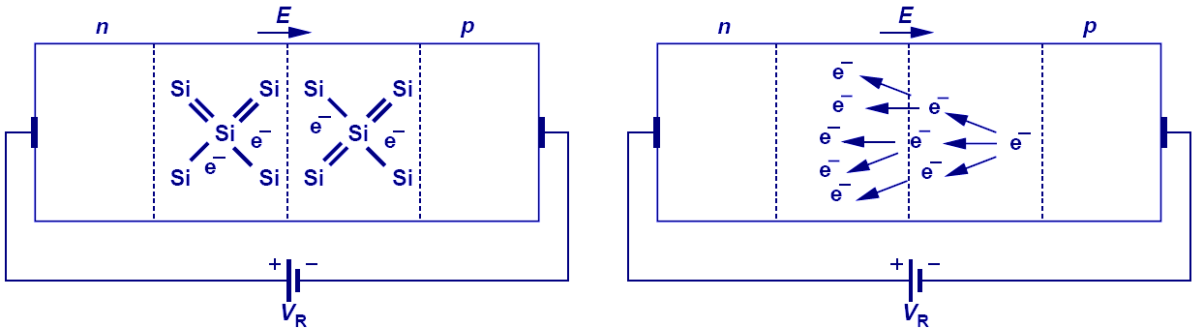
- The minority carriers, under reverse biased conditions, flowing through the junction acquire a kinetic energy which increases with the increase in reverse voltage. At a sufficiently high reverse voltage (say 5 V or more), the kinetic energy of minority carriers becomes so large that they knock out electrons from the covalent bonds of the semiconductor material. As a result of collision, the liberated electrons in turn liberate more electrons and the current becomes very large leading to the breakdown of the crystal structure itself. This phenomenon is called the avalanche breakdown. *The breakdown* region is the knee of the characteristic curve. Now the current is not controlled by the junction voltage but rather by the external circuit.

Zener breakdown

- Under a very high reverse voltage, the depletion region expands and the potential barrier increases leading to a very high electric field across the junction. The electric field will break some of the covalent bonds of the semiconductor atoms leading to a large number of free minority carriers, which suddenly increase the reverse current. This is called the Zener effect.

- The breakdown occurs at a particular and constant value of reverse voltage called the breakdown voltage, it is found that Zener breakdown occurs at electric field intensity of about 3 x 107 V/m.

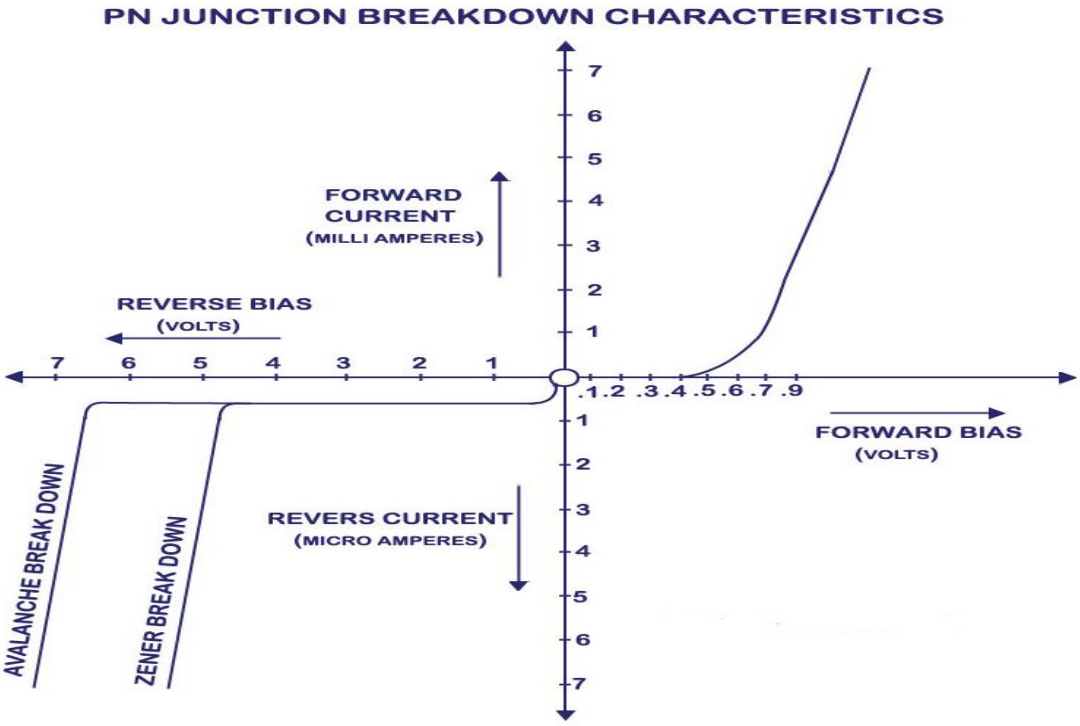
Zener vs Avalanche Breakdown:



(a) (b)

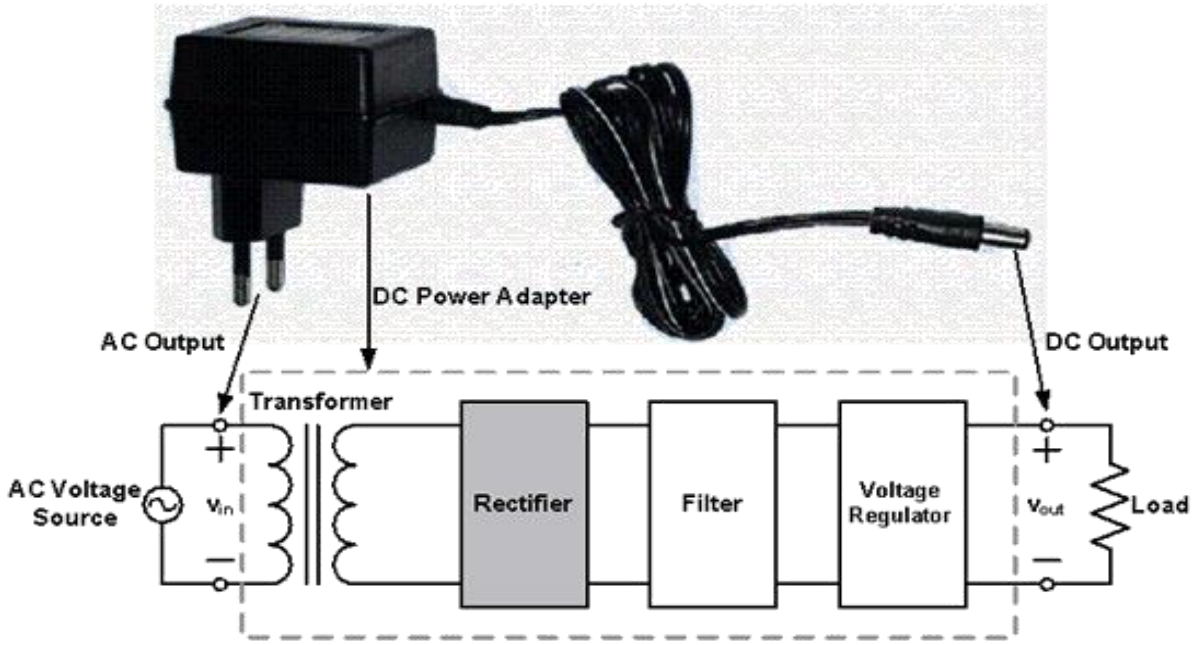
- Zener breakdown is a result of the large electric field inside the depletion region that breaks electrons or holes off their covalent bonds.
- Avalanche breakdown is a result of electrons or holes colliding with the fixed ions inside the depletion region.

BREAK DOWN MECHANISMS



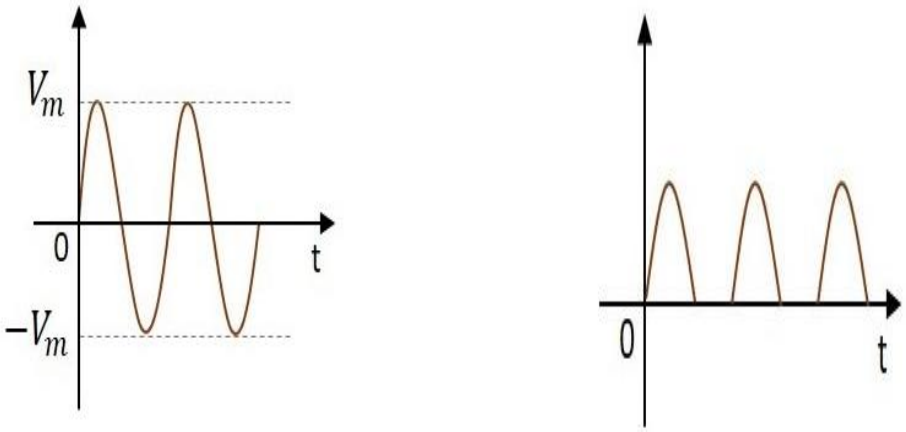
RECTIFIERS:

Block Diagram of Regulated power Supply



Rectification:

- Rectification is a process of converting the alternating quantity (voltage or current) into a corresponding direct quantity(voltage or current).

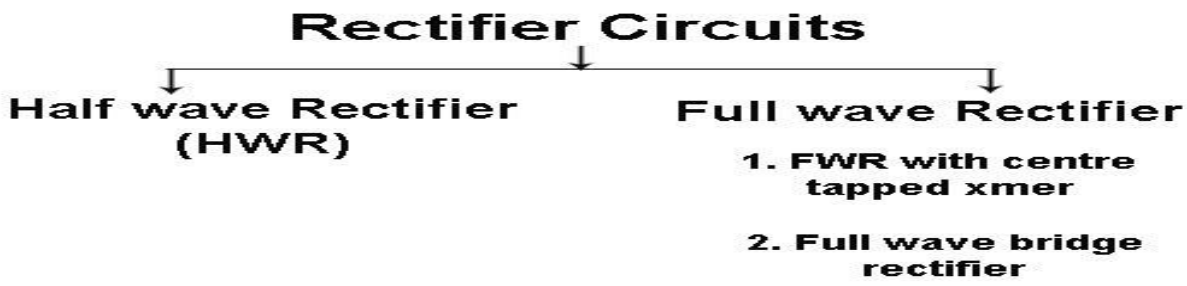


- The input to a rectifier is AC whereas its output is unidirectional or DC.

Need of Rectification

- Every electronic circuit such as amplifiers, needs a DC power source for its operation.
- This DC voltage has to be obtained from AC supply.

- For this the AC supply has to be reduced Stepped down first using a Step down transformer and then converted to dc by using rectifier.

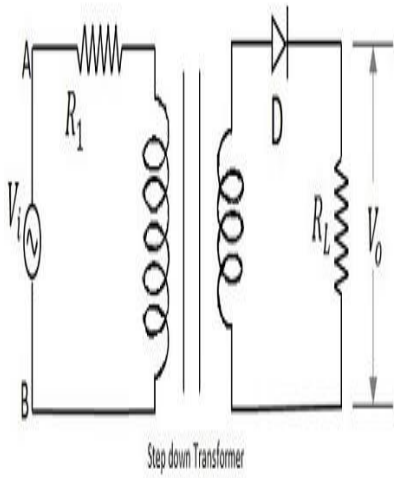


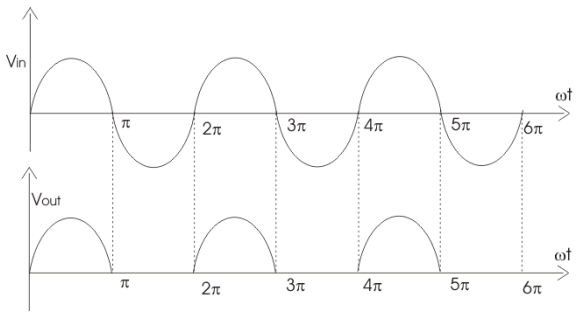
Half Wave Rectifier:

Operation:

- A Half-wave rectifier circuit rectifies only positive half cycles of the input supply .
- The AC signal is given through an input transformer which steps up or down according to the usage. Mostly a step down transformer is used in rectifier circuits, so as to reduce the input voltage.
- The input signal given to the transformer is passed through a PN junction diode which acts as a rectifier. This diode converts the AC voltage into pulsating dc for only the positive half cycles of the input. A load resistor is connected at the end of the circuit.
- This diode gets ON conducts for positive half cycles of input signal. Hence a current flows in the circuit and there will be a voltage drop across the load resistor. This output will be pulsating DC which is taken across the load resistor.

The diode gets OFF doesn′t conduct for negative half cycles and hence the output for negative half cycles will be, iD=0 and Vo=0





Analysis of Half-Wave Rectifier:

To analyze a half-wave rectifier circuit, let us consider the equation of input voltage.

$$v_i = V_m \sin \omega t$$

V_m is the maximum value of supply voltage.

Let us assume that the diode is ideal.

- The resistance in the forward direction, i.e., in the ON state is R_f .
- The resistance in the reverse direction, i.e., in the OFF state is R_r .

The current **i** in the diode or the load resistor R_L is given by

$$i = I_m \sin \omega t \quad for \quad 0 \leq \omega t \leq 2\pi$$

$$i = 0 \quad for \quad \pi \leq \omega t \leq 2\pi$$

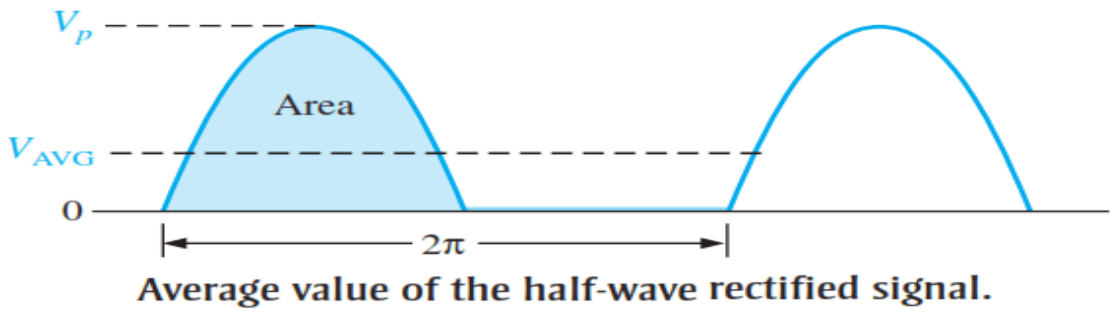
Where

$$I_m = \frac{V_m}{R_f + R_L}$$

DC Output Current:

- The average current I_{dc} is given by

$$I_{dc} = \frac{Area\ under\ the\ curve\ over\ the\ full\ cycle}{Base}$$



Average value of the half-wave rectified signal.

DC Output Current

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} i\, d(\omega t)$$

$$= \frac{1}{2\pi}\left[\int_0^{\pi} I_m \sin\omega t\, d(\omega t) + \int_0^{2\pi} 0\, d(\omega t)\right]$$

$$= \frac{1}{2\pi}[I_m\{-\cos\omega t\}_0^{\pi}]$$

$$= \frac{1}{2\pi}[I_m\{+1-(-1)\}] = \frac{I_m}{\pi} = 0.318 I_m$$

Substituting the value of I_m , we get

$$I_{dc} = \frac{V_m}{\pi(R_f + R_L)}$$

If $R_L >> R_f$, then

$$I_{dc} = \frac{V_m}{\pi R_L} = 0.318\frac{V_m}{R_L}$$

DC Output Voltage:

The DC output voltage is given by

$$V_{dc} = I_{dc} \times R_L = \frac{I_m}{\pi} \times R_L$$

$$= \frac{V_m \times R_L}{\pi(R_f + R_L)} = \frac{V_m}{\pi\{1 + (R_f/R_L)\}}$$

If $R_L >> R_f$, then

$$V_{dc} = \frac{V_m}{\pi} = 0.318 V_m$$

RMS Current and Voltage:

The value of RMS current is given by

$$I_{rms} = \left[\frac{1}{2\pi}\int_0^{2\pi} i^2 d\,(\omega t)\right]^{\frac{1}{2}}$$

$$I_{rms} = \left[\frac{1}{2\pi}\int_0^{2\pi} I_m^2 \sin^2 \omega t\, d\,(\omega t) + \frac{1}{2\pi}\int_\pi^{2\pi} 0\, d\,(\omega t)\right]^{\frac{1}{2}}$$

$$= \left[\frac{I_m^2}{2\pi}\int_0^{\pi} \left(\frac{1-\cos 2\omega t}{2}\right) d\,(\omega t)\right]^{\frac{1}{2}}$$

$$= \left[\frac{I_m^2}{4\pi}\left\{(\omega t) - \frac{\sin 2\omega t}{2}\right\}_0^{\pi}\right]^{\frac{1}{2}}$$

$$= \left[\frac{I_m^2}{4\pi}\left\{\pi - 0 - \frac{\sin 2\pi}{2} + \sin 0\right\}\right]^{\frac{1}{2}}$$

$$= \left[\frac{I_m^2}{4\pi}\right]^{\frac{1}{2}} = \frac{I_m}{2}$$

RMS voltage across the load is

$$V_{rms} = I_{rms} \times R_L = \frac{V_m \times R_L}{2\,(R_f + R_L)}$$

$$= \frac{V_m}{2\,\{1 + (R_f/R_L)\}}$$

If $R_L >> R_f$, then

$$V_{rms} = \frac{V_m}{2}$$

Rectifier Efficiency:

Any circuit needs to be efficient in its working for a better output. To calculate the efficiency of a half wave rectifier, the ratio of the output power to the input power has to be considered.

The rectifier efficiency is defined as

$$\eta = \frac{d.c.\,power\ \ delivered\ \ to\ \ the\ \ load}{a.c.\,input\ \ power\ \ from\ \ transformer\ \ secondary} = \frac{P_{ac}}{P_{dc}}$$

Now

$$P_{dc} = (I_{dc})^2 \times R_L = \frac{I_m R_L}{\pi^2}$$

Further

$$P_{ac} = P_a + P_r$$

Where

$$P_a = power\ dissipated\ at\ the\ junction\ of\ diode$$

$$= I_{rms}^2 \times R_f = \frac{I_m^2}{4} \times R_f$$

And

$$P_r = power\ dissipated\ in\ the\ load\ resistance$$

$$= I_{rms}^2 \times R_L = \frac{I_m^2}{4} \times R_L$$

$$P_{ac} = \frac{I_m^2}{4} \times R_f + \frac{I_m^2}{4} \times R_L = \frac{I_m^2}{4}(R_f + R_L)$$

From both the expressions of P_{ac} and P_{dc}, we can write

$$\eta = \frac{I_m^2 R_L/\pi^2}{I_m^2 (R_f + R_L)/4} = \frac{4}{\pi^2} \frac{R_L}{(R_f + R_L)}$$

$$= \frac{4}{\pi^2} \frac{1}{\{1 + (R_f/R_L)\}} = \frac{0.406}{\{1 + (R_f/R_L)\}}$$

Percentage rectifier efficiency

$$\eta = \frac{40.6}{\{1 + (R_f/R_L)\}}$$

Ripple Factor:

- The rectified output contains some amount of AC component present in it, in the form of ripples. This is understood by observing the output waveform of the half wave rectifier. To get a pure dc, we need to have an idea on this component.
- The ripple factor gives the waviness of the rectified output. It is denoted by **y**. This can be defined as the ratio of the effective value of ac component of voltage or current to the direct value or average value.

$$\gamma = \frac{ripple\ voltage}{d.c\ voltage} = \frac{rms\ value\ of\ a.c.component}{d.c.value\ of\ wave} = \frac{(V_r)_{rms}}{v_{dc}}$$

Here,

$$(V_r)_{rms} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

Therefore,

$$\gamma = \frac{\sqrt{V_{rms}^2 - V_{dc}^2}}{V_{dc}} = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

Now,

$$V_{rms} = \left[\frac{1}{2\pi}\int_0^{2\pi} V_m^2 \sin^2 \omega t\, d(\omega t)\right]^{\frac{1}{2}}$$

$$= V_m\left[\frac{1}{4\pi}\int_0^{\pi} (1 - \cos 2\,\omega t)\, d(\omega t)\right]^{\frac{1}{2}} = \frac{V_m}{2}$$

$$V_{dc} = V_{av} = \frac{1}{2\pi}\left[\int_0^{\pi} V_m \sin \omega t\, d(\omega t) + \int_0^{2\pi} 0.d(\omega t)\right]$$

$$= \frac{V_m}{2\pi}[-\cos \omega t]_0^{\pi} = \frac{V_m}{\pi}$$

$$\gamma = \sqrt{\left[\left\{\frac{(V_m/2)}{(V_m/\pi)}\right\}^2 - 1\right]} = \sqrt{\left\{\left(\frac{\pi}{2}\right)^2 - 1\right\}} = 1.21$$

The ripple factor is also defined as

$$\gamma = \frac{(I_r)_{rms}}{I_{dc}}$$

As the value of ripple factor present in a half wave rectifier is 1.21, it means that the amount of a.c. present in the output is 121% of the d.c. voltage

Regulation:

- The current through the load may vary depending upon the load resistance. But even at such condition, we expect our output voltage which is taken across that load resistor, to be constant. So, our voltage needs to be regulated even under different load conditions.
- The variation of D.C. output voltage with change in D.C. load current is defined as the **Regulation**.

- The lower the percentage regulation, the better would be the power supply. An ideal power supply will have a zero percentage regulation.
- The percentage regulation is calculated as follows.

$$Percentage\ regulation = \frac{V_{no\ load} - V_{full\ load}}{V_{full\ load}} \times 100\%$$

Transformer Utilization Factor:

The D.C. power to be delivered to the load, in a rectifier circuit decides the rating of the transformer used in a circuit.

So, the transformer utilization factor is defined as

$$TUF = \frac{d.c.\ power\ to\ be\ delivered\ to\ the\ load}{a.c.\ rating\ of\ the\ transformer\ secondary}$$

$$= \frac{P_{d.c}}{P_{a.c(rated)}}$$

According to the theory of transformer, the rated voltage of the secondary will be

$$V_m/\sqrt{2}$$

The actual R.M.S. voltage flowing through it will be

$$I_m/2$$

Therefore

$$TUF = \frac{(I_m/\pi)^2 \times R_L}{(V_m/\sqrt{2}) \times (I_m/2)}$$

But

$$V_m = I_m\ (R_f + R_L)$$

Therefore

$$TUF = \frac{(I_m/\pi)^2 \times R_L}{\{I_m\ (R_f + R_L)/\sqrt{2}\} \times (I_m/2)}$$

$$= \frac{2\sqrt{2}}{\pi^2} \times \frac{R_L}{(R_f + R_L)}$$

$$= \frac{2\sqrt{2}}{\pi^2} = 0.287$$

Peak Inverse Voltage:

- A diode when connected in reverse bias, should be operated under a controlled level of voltage. If that safe voltage is exceeded, the diode gets damaged. Hence it is very important to know about that maximum voltage.

- The maximum inverse voltage that the diode can withstand without being destroyed is called as **Peak Inverse Voltage**. In short, **PIV**.
- Here the PIV is nothing but Vm

Form Factor:

- This can be understood as the mathematical mean of absolute values of all points on the waveform. The **form factor** is defined as the ratio of R.M.S. value to the average value. It is denoted by **F**.

$$F = \frac{rms\ value}{average\ value} = \frac{I_m/2}{I_m/\pi} = \frac{0.5I_m}{0.318I_m} = 1.57$$

Peak Factor:

- The value of peak in the ripple has to be considered to know how effective the rectification is. The value of peak factor is also an important consideration. **Peak factor** is defined as the ratio of peak value to the R.M.S. value.
- Therefore

$$PeakFactor = \frac{Peak\ value}{r.m.s\ value} = \frac{V_m}{V_m/2} = 2$$

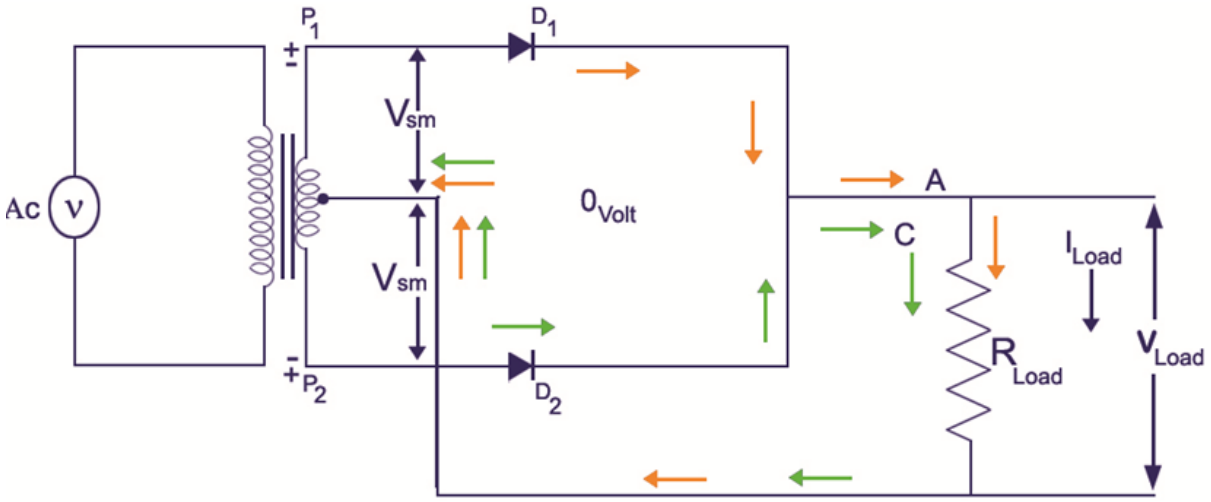
Full-Wave Rectifier:

- A Rectifier circuit that rectifies both the positive and negative half cycles can be termed as a full wave rectifier as it rectifies the complete cycle. The construction of a full wave rectifier can be made in two types. They are
- Center-tapped Full wave rectifier
- Bridge full wave rectifier

Center-tapped Full-Wave Rectifier:

- A rectifier circuit whose transformer secondary is tapped to get the desired output voltage, using two diodes alternatively, to rectify the complete cycle is called as a **Center-tapped Full wave rectifier circuit**.

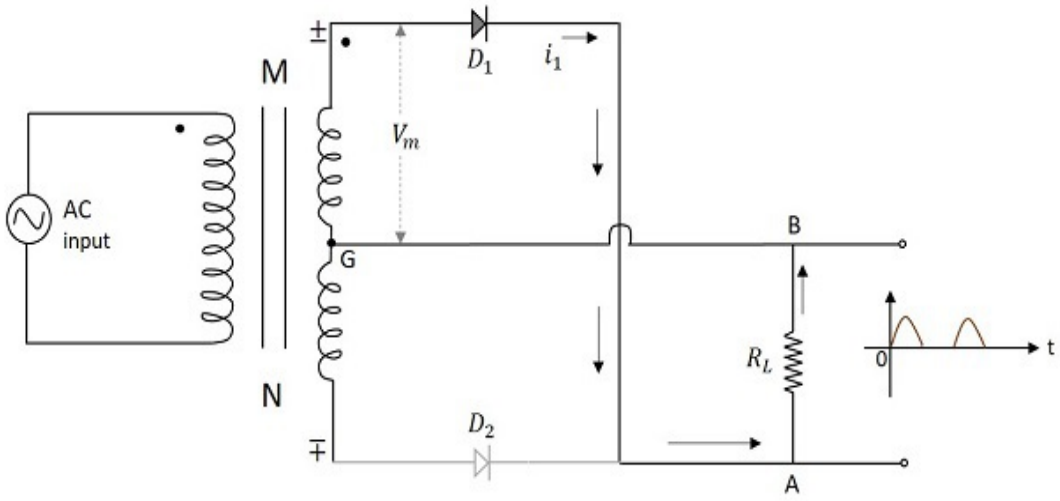
- The features of a center-tapping transformer are −
- The tapping is done by drawing a lead at the mid-point on the secondary winding. This winding is split into two equal halves by doing so.
- The voltage at the tapped mid-point is zero. This forms a neutral point.
- The center tapping provides two separate output voltages which are equal in magnitude but opposite in polarity to each other.
- A number of tapings can be drawn out to obtain different levels of voltages.



CENTRE - TAP FULL- WAVE RECTIFIER CIRCUIT

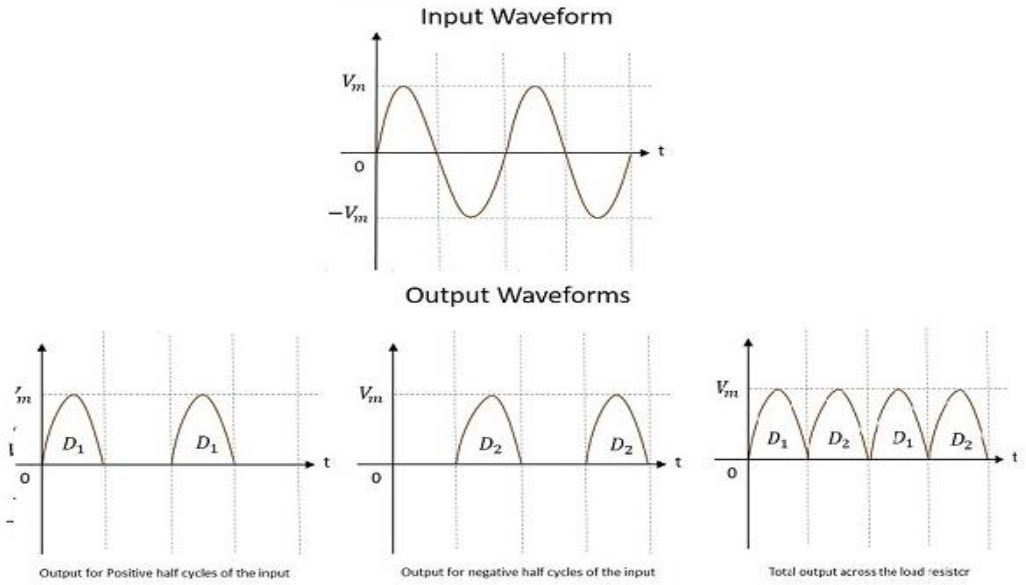
Working:

The working of a center-tapped full wave rectifier can be understood by the above figure. When the positive half cycle of the input voltage is applied, the point M at the transformer secondary becomes positive with respect to the point N. This makes the diode D_1 forward biased. Hence current i_1 flows through the load resistor from A to B. We now have the positive half cycles in the output



Waveforms of CT FWR:

The input and output waveforms of the center-tapped full wave rectifier are as follows.



From the above figure it is evident that the output is obtained for both the positive and negative half cycles. It is also observed that the output across the load resistor is in the **same direction** for both the half cycles.

Peak Inverse Voltage:

- As the maximum voltage across half secondary winding is V_m, the whole of the secondary voltage appears across the non-conducting diode. Hence the **peak inverse voltage** is twice the maximum voltage across the half-secondary winding, i.e.

$$PIV = 2V_m$$

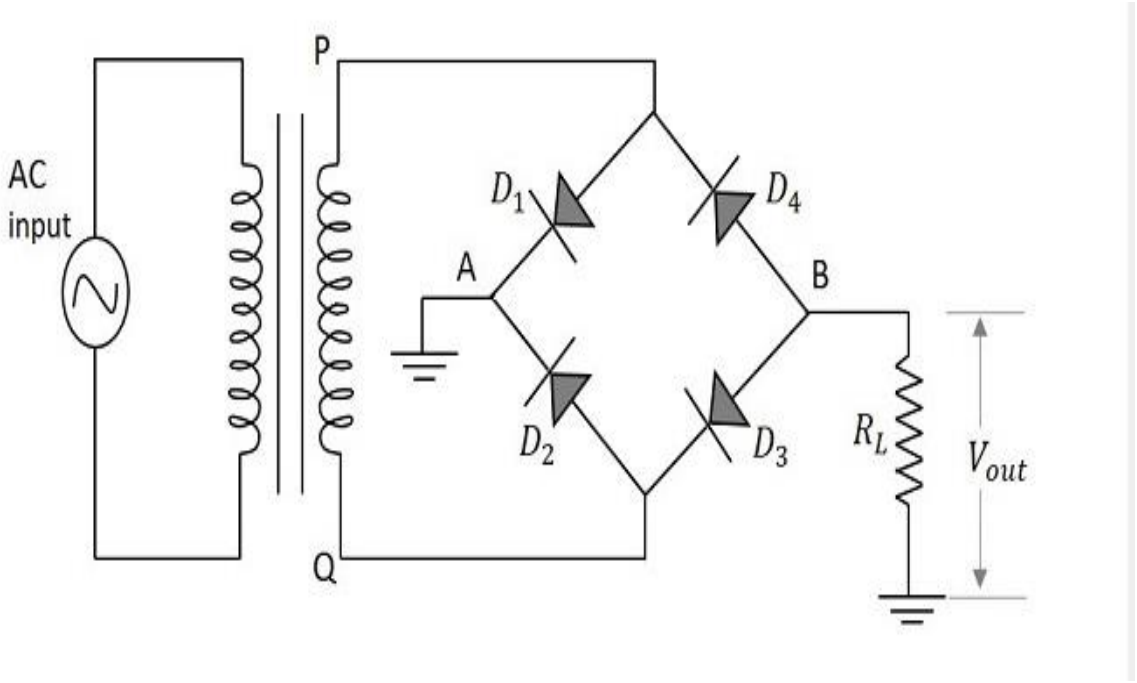
Disadvantages:

- There are few disadvantages for a center-tapped full wave rectifier such as −
- Location of center-tapping is difficult
- The dc output voltage is small
- PIV of the diodes should be high

Bridge Full-Wave Rectifier:

- It utilizes four diodes connected in bridge form so as not only to produce the output during the full cycle of input, but also to eliminate the disadvantages of the center-tapped full wave rectifier circuit.

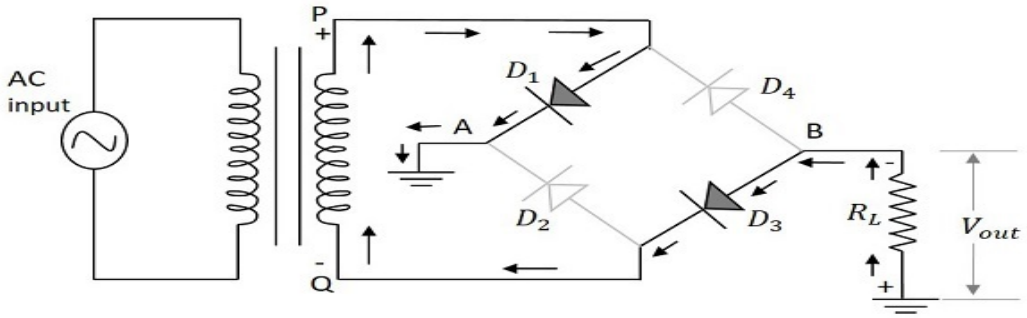
- There is no need of any center-tapping of the transformer in this circuit. Four diodes called D_1, D_2, $D_3$and D_4 are used in constructing a bridge type network so that two of the diodes conduct for one half cycle and two conduct for the other half cycle of the input supply.



Working:

The full wave rectifier with four diodes connected in bridge circuit is employed to get a better full wave output response. When the positive half cycle of the input supply is given, point P becomes positive with respect to the point **Q**. This makes the diode D_1 and D_3 forward biased while D_2 and D_4 reverse biased. These two diodes will now be in series with the load resistor.

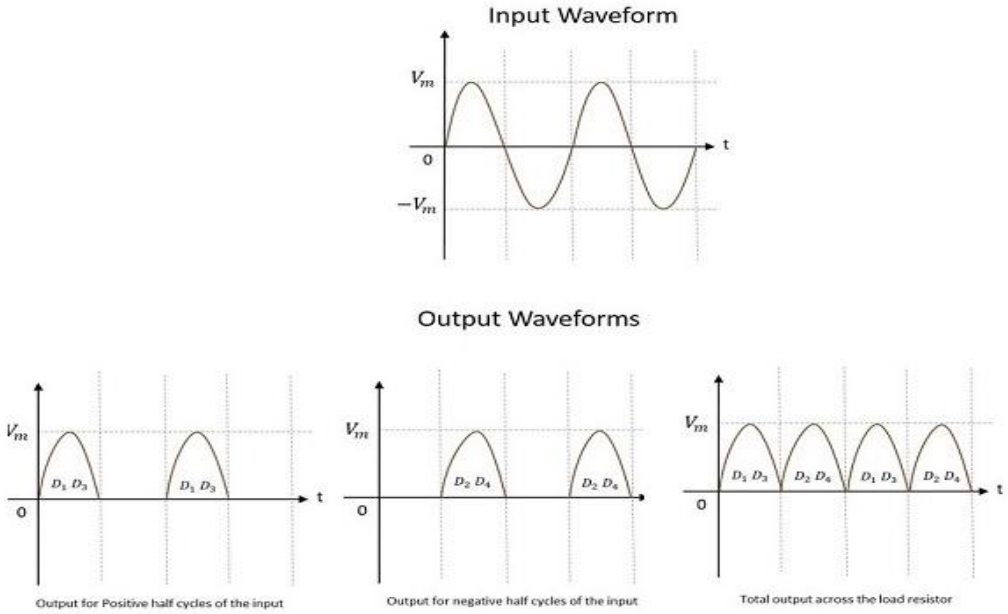
The following figure indicates this along with the conventional current flow in the circuit.



- Hence the diodes D_2 and D_4 conduct during the negative half cycle of the input supply to produce the output along the load resistor. Here also two diodes work to produce the output voltage. The current flows in the same direction as during the positive half cycle of the input.

Waveforms:

The input and output waveforms of the center-tapped full wave rectifier are as follows.



From the above figure, it is evident that the output is obtained for both the positive and negative half cycles. It is also observed that the output across the load resistor is in the **same direction** for both the half cycles.

Peak Inverse Voltage:

- Whenever two of the diodes are being in parallel to the secondary of the transformer, the maximum secondary voltage across the transformer appears at the non-conducting diodes which makes the PIV of the rectifier circuit. Hence the **peak inverse voltage** is the maximum voltage across the secondary winding, i.e.

$$PIV = V_m$$

Advantages:

- There are many advantages for a bridge full wave rectifier, such as −
- No need of center-tapping.
- The dc output voltage is twice that of the center-tapper FWR.
- PIV of the diodes is of the half value that of the center-tapper FWR.
- The design of the circuit is easier with better output.

Analysis:

In order to analyze a full wave rectifier circuit, let us assume the input voltage V_i as,

$$V_i = V_m \sin \omega t$$

The current i_1 through the load resistor R_L is given by

$$i_1 = I_m \sin \omega t \quad for \quad 0 \leq \omega t \leq \pi$$

$$i_1 = \quad 0 \qquad for \quad \pi \leq \omega t \leq 2\pi$$

Where

$$I_m = \frac{V_m}{R_f + R_L}$$

R_f being the diode resistance in ON condition.

Similarly, the current i_2 flowing through diode D_2 and load resistor RL is given by,

$$i_2 = \quad 0 \qquad for \quad 0 \leq \omega t \leq \pi$$

$$i_2 = I_m \sin \omega t \quad for \quad \pi \leq \omega t \leq 2\pi$$

The total current flowing through R_L is the sum of the two currents i_1 and i_2 i.e.

$$i = i_1 + i_2$$

D.C. or Average Current:

The average value of output current that a D.C. ammeter will indicate is given by

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} i_1 \, d(\omega t) + \frac{1}{2\pi}\int_0^{2\pi} i_2 \, d(\omega t)$$

$$= \frac{1}{2\pi \int_0^{\pi}} I_m \sin\omega t \, d(\omega t) + 0 + 0 +$$

$$\frac{1}{2\pi}\int_0^{2\pi} I_m \sin\omega t \, d(\omega t)$$

$$= \frac{I_m}{\pi} + \frac{I_m}{\pi} = \frac{2I_m}{\pi} = 0.636 I_m$$

This is double the value of a half wave rectifier.

D.C. Output Voltage:

The dc output voltage across load is given by

$$V_{dc} = I_{dc} \times R_L = \frac{2I_m R_L}{\pi} = 0.636 I_m R_L$$

Thus the dc output voltage is twice that of a half wave rectifier.

RMS Current:

The RMS value of the current is given by

$$I_{rms} = \left[\frac{1}{\pi}\int_0^{\pi} t^2\, d(\omega t)\right]^{\frac{1}{2}}$$

Since current is of the two same form in the two halves

$$= \left[\frac{I_m^2}{\pi}\int_0^{\pi} \sin^2 \omega t\, d(\omega t)\right]^{\frac{1}{2}}$$

$$= \frac{I_m}{\sqrt{2}}$$

Rectifier Efficiency:

The rectifier efficiency is defined as

$$\eta = \frac{P_{dc}}{P_{ac}}$$

Now,

$$P_{dc} = (V_{dc})^2/R_L = (2V_m/\pi)^2$$

And,

$$P_{ac} = (V_{rms})^2/R_L = (V_m/\sqrt{2})^2$$

Therefore,

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{(2V_m/\pi)^2}{(V_m/\sqrt{2})^2} = \frac{8}{\pi^2}$$

$$= 0.812 = 81.2\%$$

Ripple Factor:

The form factor of rectified output voltage of a full wave rectifier is given by

$$F = \frac{I_{rms}}{I_{dc}} = \frac{I_m/\sqrt{2}}{2I_m/\pi} = 1.11$$

The ripple factor γ is defined as $usingaccircuittheory$

$$\gamma = \left[\left(\frac{I_{rms}}{I_{dc}}\right) - 1\right]^{\frac{1}{2}} = (F^2 - 1)^{\frac{1}{2}}$$

$$= \left[(1.11)^2 - 1\right]^{\frac{1}{2}} = 0.48$$

This is a great improvement over the half wave rectifier's ripple factor which was 1.21

Regulation:

The dc output voltage is given by

$$V_{dc} = \frac{2I_m R_L}{\pi} = \frac{2V_m R_L}{\pi(R_f + R_L)}$$

$$= \frac{2V_m}{\pi}\left[1 - \frac{R_f}{R_f + R_L}\right] = \frac{2V_m}{\pi} - I_{dc}R_f$$

Transformer Utilization Factor:

The TUF of a half wave rectifier is 0.287

There are two secondary windings in a center-tapped rectifier and hence the TUF of centertapped full wave rectifier is

$$(TUF)_{avg} = \frac{P_{dc}}{V - A\,rating\,of\,a\,transformer}$$

$$= \frac{(TUF)_p + (TUF)_s + (TUF)_s}{3}$$

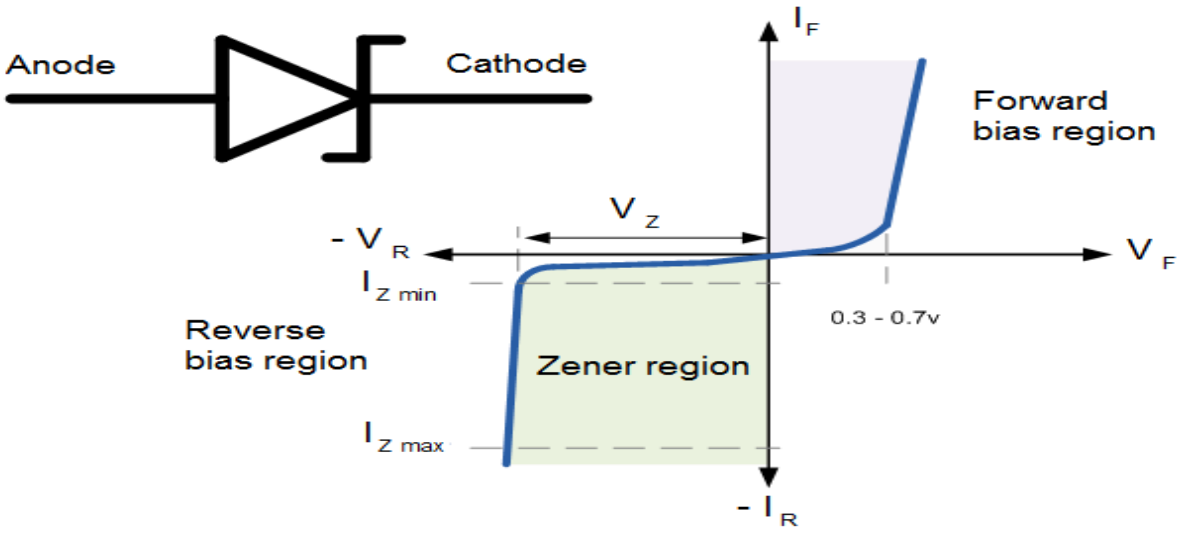
$$= \frac{0.812 + 0.287 + 0.287}{3} = 0.693$$

Terms	Half Wave Rectifier	Center Tapped FWR	Bridge FWR
Number of Diodes	1	2	4
Transformer tapping	No	Yes	No
Peak Inverse Voltage	V_m	$2V_m$	V_m
Maximum Efficiency	40.6%	81.2%	81.2%
Average / dc current	I_m/π	$2I_m/\pi$	$2I_m/\pi$
DC voltage	V_m/π	$2V_m/\pi$	$2V_m/\pi$
RMS current	$I_m/2$	$I_m/\sqrt{2}$	$I_m/\sqrt{2}$
Ripple Factor	1.21	0.48	0.48
Output frequency	f_{in}	$2f_{in}$	$2f_{in}$

ZENER DIODE :

- The Zener diode is like a general-purpose signal diode consisting of a silicon PN junction.
- When biased in the forward direction it behaves just like a normal signal diode passing the rated current, but as soon as a reverse voltage applied across the zener diode exceeds the rated voltage of the device, the diodes breakdown voltage VB is reached at which point a process called *Avalanche Breakdown occurs in the* semiconductor depletion layer and a current starts to flow through the diode to limit this increase in voltage.
- The current now flowing through the zener diode increases dramatically to the maximum circuit value (which is usually limited by a series resistor) and once achieved this reverse saturation current remains fairly constant over a wide range of applied voltages. This breakdown voltage point, VB is called the "zener voltage" for zener diodes and can range from less than one volt to hundreds of volts.

Symbol and V-I Characteristics:



The dynamic resistance of Zener diode is given by

$$r_z = \Delta Vz / \Delta Iz$$

- The point at which the zener voltage triggers the current to flow through the diode can be very accurately controlled (to less than 1% tolerance) in the doping stage of the diodes semiconductor construction giving the diode a specific *zener breakdown voltage, (Vz) for example, 4.3V or 7.5V.*
- *This* zener breakdown voltage on the I-V curve is almost a vertical straight line.
- The Zener Diode is used in its "reverse bias" or reverse breakdown mode, i.e. the diodes anode connects to the negative supply.

- From the I-V characteristics curve above, we can see that the zener diode has a region in its reverse bias characteristics of almost a constant negative voltage regardless of the value of the current flowing through the diode and remains nearly constant even with large changes in current as long as the zener diodes current remains between the breakdown current IZ(min) and the maximum current rating IZ(max).
- This ability to control itself can be used to great effect to regulate or stabilize a voltage source against supply or load variations. The fact that the voltage across the diode in the breakdown region is almost constant turns out to be an important application of the zener diode as a voltage regulator.

The function of a regulator is to provide a constant output voltage to a load connected in parallel with it in spite of the ripples in the supply voltage or the variation in the load current and the zener diode will continue to regulate the voltage until the diodes current falls below the minimum IZ(min) value in the reverse breakdown region. Applications:

- Zener diodes are used in Voltage stabilizers (or) shunt regulators
- used in Surge suppression circuitry for device protection
- used in Over voltage protection circuits.
- Zener diodes are used in clipping and clamping circuits especially peak clippers .
- They are used as Reference elements.
- Used in switching applications.

Clamper Circuits:

- A Clamper Circuit is a circuit that adds a DC level to an AC signal. Actually, the positive and negative peaks of the signals can be placed at desired levels using the clamping circuits. As the DC level gets shifted, a clamper circuit is called as a **Level Shifter**.
- Clamper circuits consist of energy storage elements like capacitors. A simple clamper circuit comprises of a capacitor, a diode, a resistor and a dc battery if required.
- A Clamper circuit can be defined as the circuit that consists of a diode, a resistor and a capacitor that shifts the waveform to a desired DC level without changing the actual appearance of the applied signal.
- A Clamper circuit can be defined as the circuit that consists of a diode, a resistor and a capacitor that shifts the waveform to a desired DC level without changing the actual appearance of the applied signal.
- In order to maintain the time period of the wave form, the τ must be greater than, half the time period discharging time of the capacitor should be slow.

$$\tau = RC$$

Where

- R is the resistance of the resistor employed
- C is the capacitance of the capacitor used
- The time constant of charge and discharge of the capacitor determines the output of a clamper circuit.
- In a clamper circuit, a vertical shift of upward or downward takes place in the output waveform with respect to the input signal.
- The load resistor and the capacitor affect the waveform. So, the discharging time of the capacitor should be large enough.
- The DC component present in the input is rejected when a capacitor coupled network is used as a capacitor blocks dc. Hence when **dc** needs to be **restored**, clamping circuit is used.

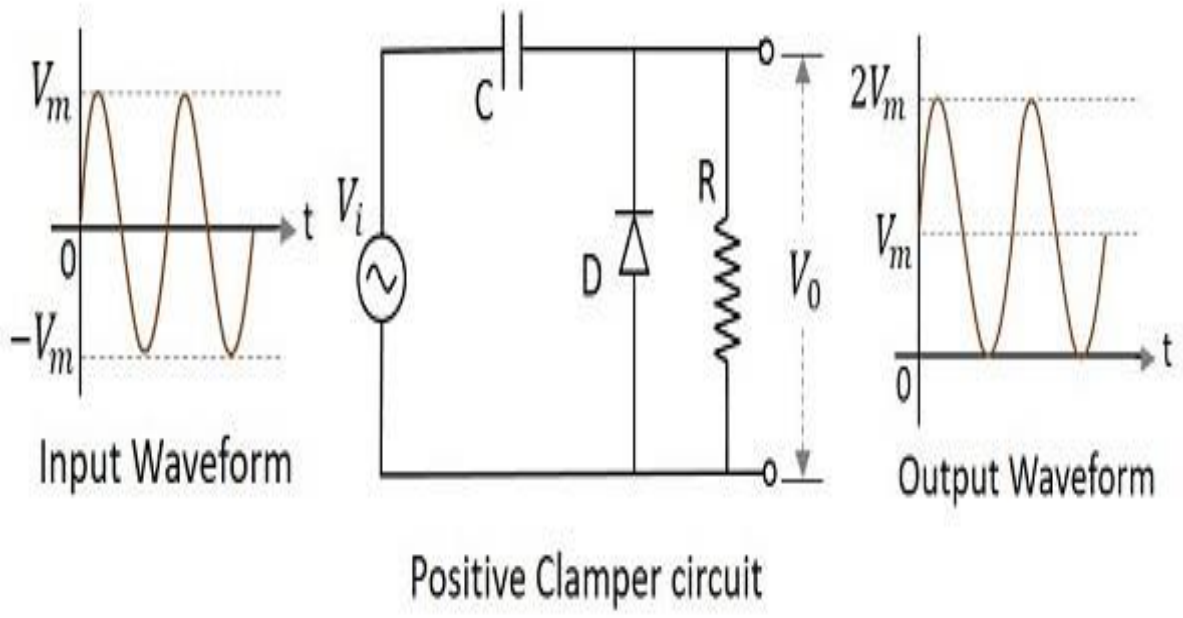
Types of Clampers:

There are few types of clamper circuits, such as

- Positive Clamper
  - ❖ Positive clamper with positive V_r
  - ❖ Positive clamper with negativeV_r
- Negative Clamper
  - ❖ Negative clamper with positive V_r
  - ❖ Negative clamper with negative V_r

Positive Clamper Circuit:

- A Clamping circuit restores the DC level. When a negative peak of the signal is raised above to the zero level, then the signal is said to be **positively clamped**.
- A Positive Clamper circuit is one that consists of a diode, a resistor and a capacitor and that shifts the output signal to the positive portion of the input signal.



Positive Clamper circuit

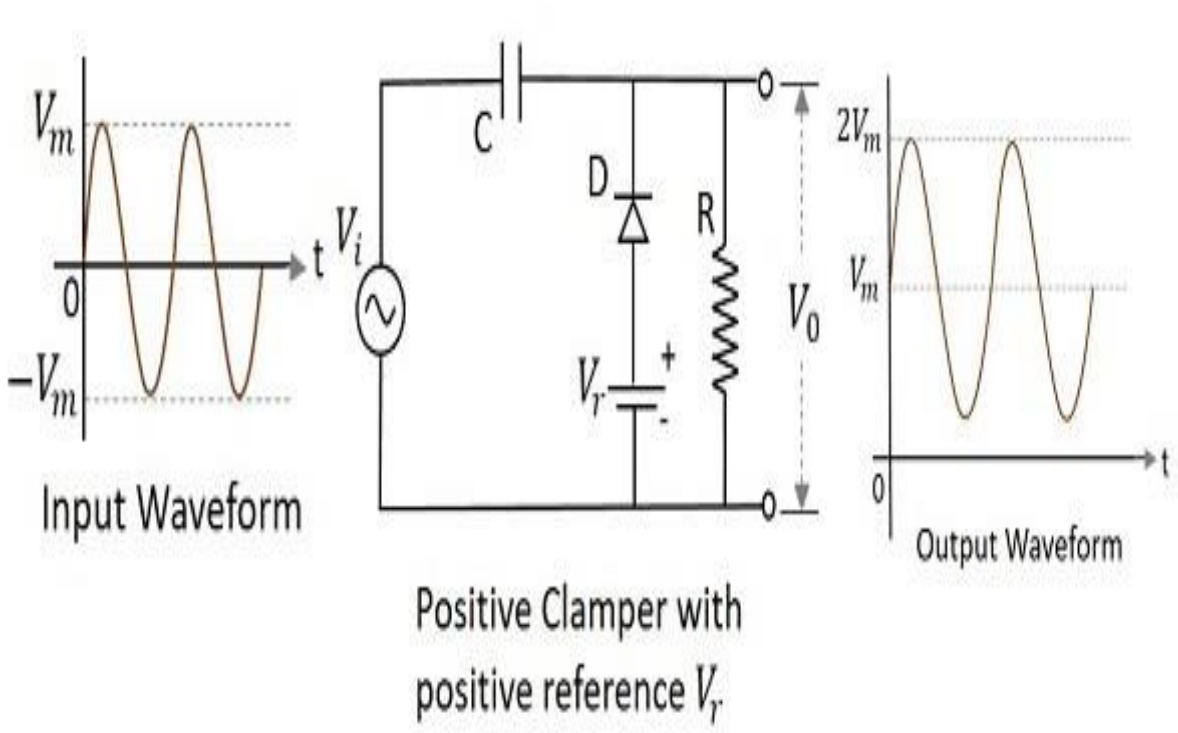
- Initially when the input is given, the capacitor is not yet charged and the diode is reverse biased. The output is not considered at this point of time.
- During the negative half cycle, at the peak value, the capacitor gets charged with negative on one plate and positive on the other. The capacitor is now charged to its peak value V_m The diode is forward biased and conducts heavily.
- During the next positive half cycle, the capacitor is charged to positive V_m while the diode gets reverse biased and gets open circuited.
- The output of the circuit at this moment will be

$$V_o=V_i+Vm$$

- The output signal changes according to the changes in the input, but shifts the level according to the charge on the capacitor, as it adds the input voltage.

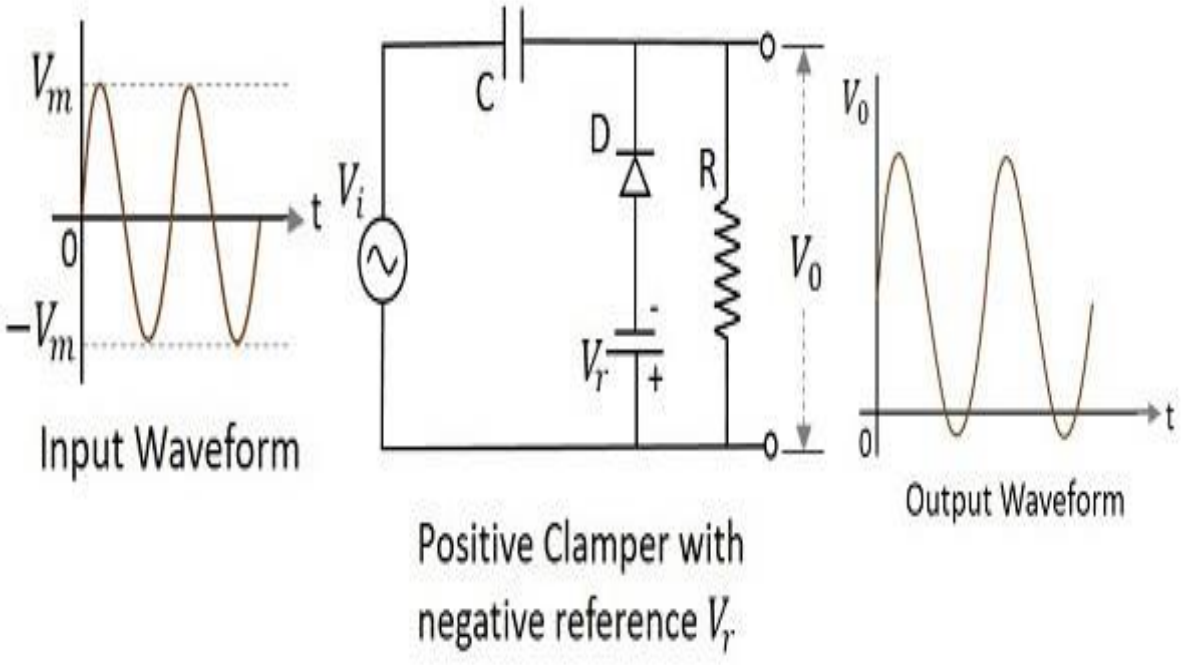
Positive Clamper with Positive V_r

- A Positive clamper circuit if biased with some positive reference voltage, that voltage will be added to the output to raise the clamped level.
- During the positive half cycle, the reference voltage is applied through the diode at the output and as the input voltage increases, the cathode voltage of the diode increase with respect to the anode voltage and hence it stops conducting.
- During the negative half cycle, the diode gets forward biased and starts conducting. The voltage across the capacitor and the reference voltage together maintain the output voltage level.



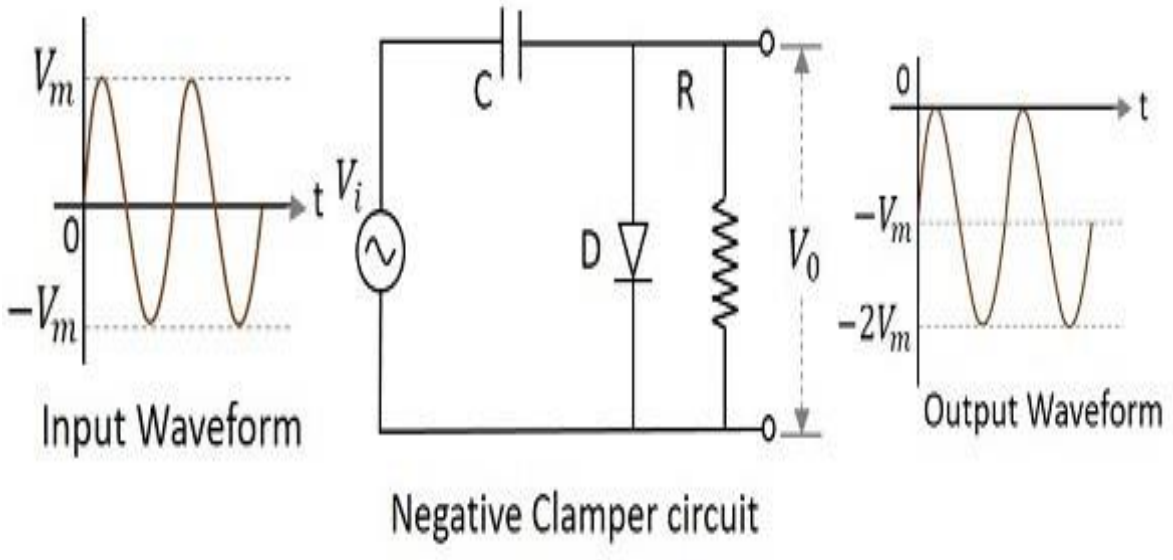
- **Positive Clamper with Negative V_r:**

- A Positive clamper circuit if biased with some negative reference voltage, that voltage will be added to the output to raise the clamped level
- During the positive half cycle, the voltage across the capacitor and the reference voltage together maintain the output voltage level.
- During the negative half-cycle, the diode conducts when the cathode voltage gets less than the anode voltage.



Negative Clamper:

- A Negative Clamper circuit is one that consists of a diode, a resistor and a capacitor and that shifts the output signal to the negative portion of the input signal.



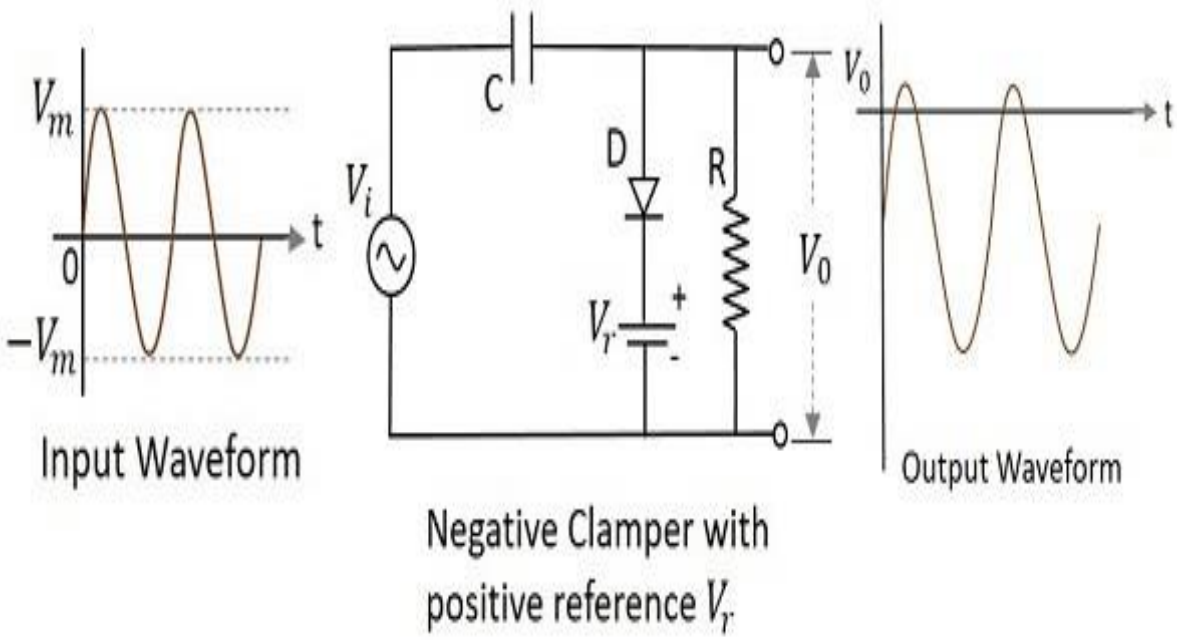
- During the positive half cycle, the capacitor gets charged to its peak value V_m . The diode is forward biased and conducts.
- During the negative half cycle, the diode gets reverse biased and gets open circuited. The output of the circuit at this moment will be

$$V_o = V_i + V_m$$

- Hence the signal is negatively clamped as shown in the above figure. The output signal changes according to the changes in the input, but shifts the level according to the charge on the capacitor, as it adds the input voltage.

Negative clamper with positive V_r

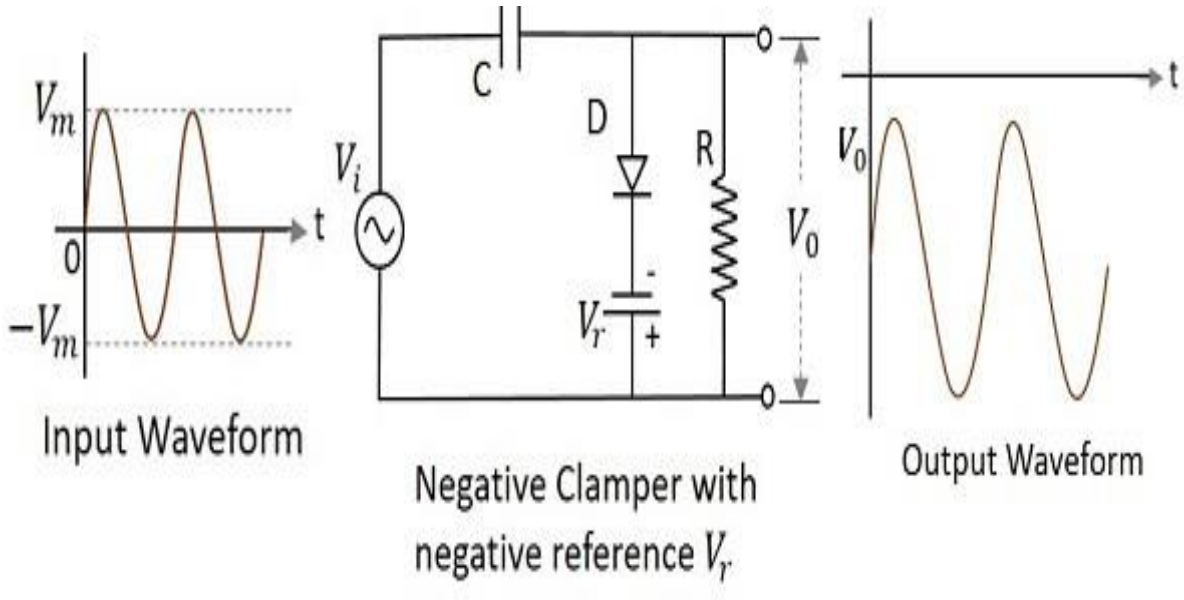
- A Negative clamper circuit if biased with some positive reference voltage, that voltage will be added to the output to raise the clamped level. Though the output voltage is negatively clamped, a portion of the output waveform is raised to the positive level, as the applied reference voltage is positive.
- During the positive half-cycle, the diode conducts, but the output equals the positive reference voltage applied.
- During the negative half cycle, the diode acts as open circuited and the voltage across the capacitor forms the output.



- **Negative Clamper with Negative V_r**

- A Negative clamper circuit if biased with some negative reference voltage, that voltage will be added to the output to raise the clamped level.
- The cathode of the diode is connected with a negative reference voltage, which is less than that of zero and the anode voltage. Hence the diode starts conducting during positive half cycle, before the zero voltage level.

During the negative half cycle, the voltage across the capacitor appears at the output. Thus the waveform is clamped towards the negative portion.



Applications:

- Used as direct current restorers
- Used to remove distortions
- Used as voltage multipliers
- Used for the protection of amplifiers
- Used as test equipment
- Used as base-line stabilizer

CLIPPING CIRCUITS:

- A Clipper circuit is a circuit that rejects the part of the input wave specified while allowing the remaining portion. The portion of the wave above or below the cut off voltage determined is clipped off or cut off.
- The clipping circuits consist of linear and non-linear elements like resistors and diodes but not energy storage elements like capacitors.

ADVANTAGES:

- To eliminate the unwanted noise present in the amplitudes.
- These can work as square wave converters, as they can convert sine waves into square waves by clipping.
- The amplitude of the desired wave can be maintained at a constant level.

TYPES:

Diode Clippers are two main types

1. **Positive clippers** and
2. **Negative clippers**

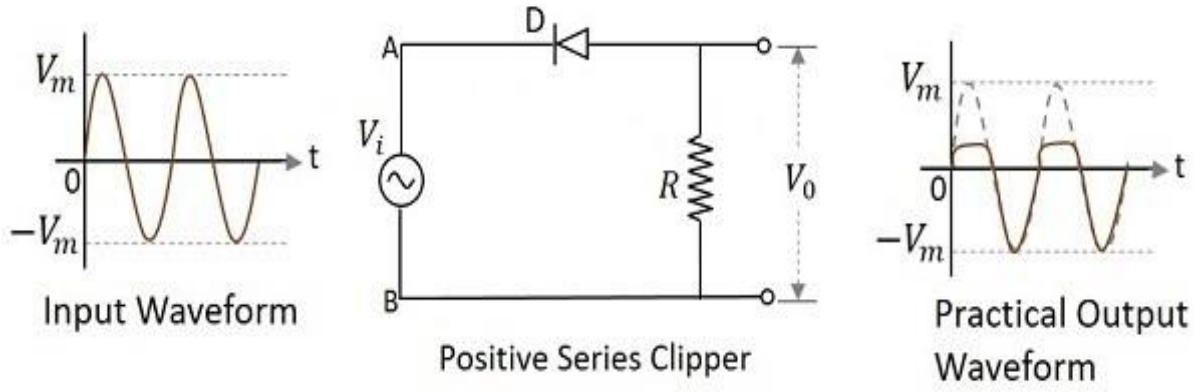
Positive clippers: The Clipper circuit that is intended to attenuate positive portions of the input signal

Among the positive diode clipper circuits, we have the following types −

- Positive Series Clipper
- Positive Series Clipper with positive V_r
- Positive Series Clipper with negative V_r
- Positive Shunt Clipper
- Positive Shunt Clipper with positive V_r
- Positive Shunt Clipper with negative V_r

POSITIVE SERIES CLIPPER

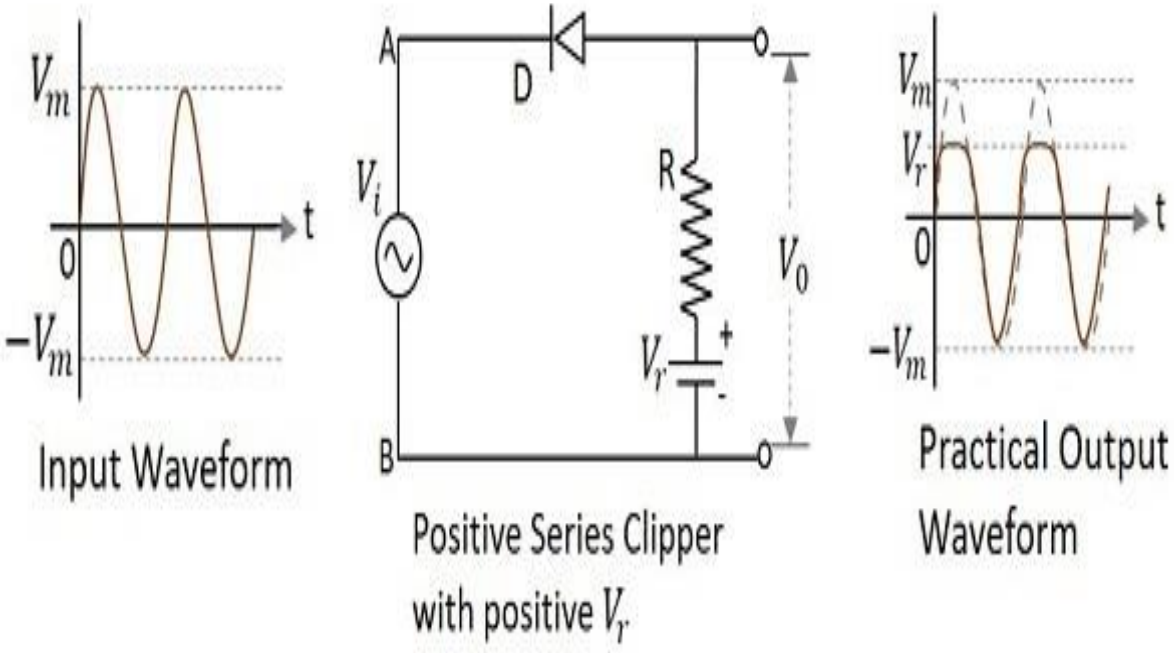
- A Clipper circuit in which the diode is connected in series to the input signal and that attenuates the positive portions of the waveform, is termed as **Positive Series Clipper**



Positive Series Clipper with positive V_r

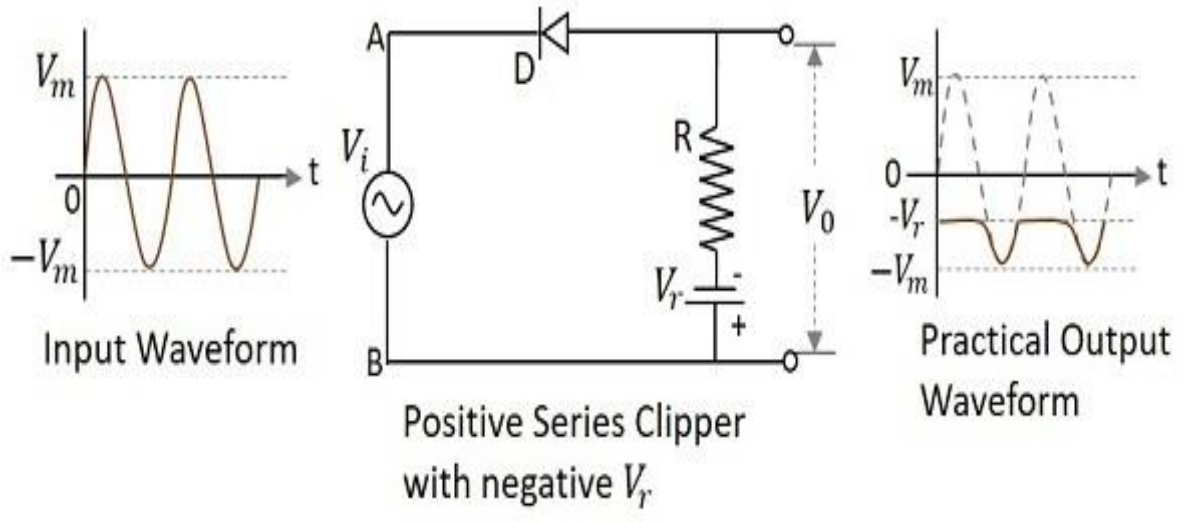
- A Clipper circuit in which the diode is connected in series to the input signal and biased with positive reference voltage V_r and that attenuates the positive portions of the waveform, is termed as **Positive Series Clipper with positive** V_r
- During the positive cycle of the input the diode gets reverse biased and the reference voltage appears at the output.

- During its negative cycle, the diode gets forward biased and conducts like a closed switch.



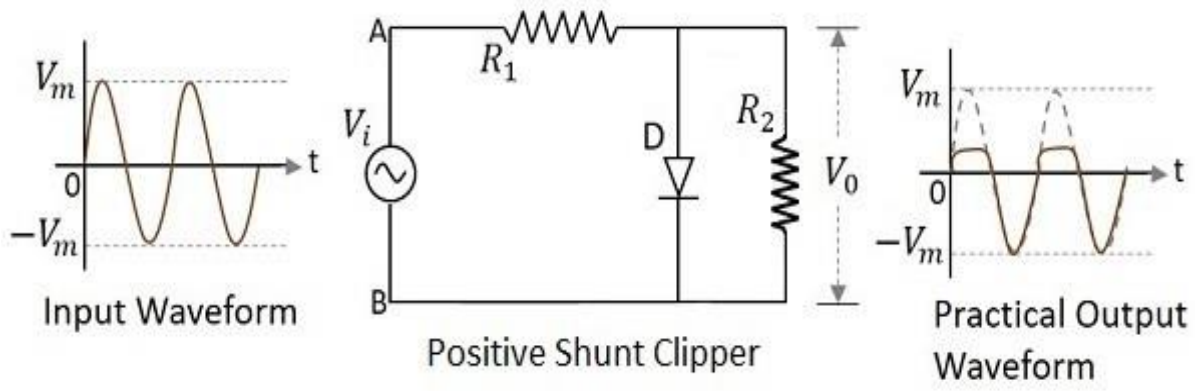
Positive Series Clipper with negative V_r

- A Clipper circuit in which the diode is connected in series to the input signal and biased with negative reference voltage V_r and that attenuates the positive portions of the waveform, is termed as **Positive Series Clipper with negative** V_r
- During the positive cycle of the input the diode gets reverse biased and the reference voltage appears at the output. As the reference voltage is negative, the same voltage with constant amplitude is shown.
- During its negative cycle, the diode gets forward biased and conducts like a closed switch. Hence the input signal that is greater than the reference voltage, appears at the output.



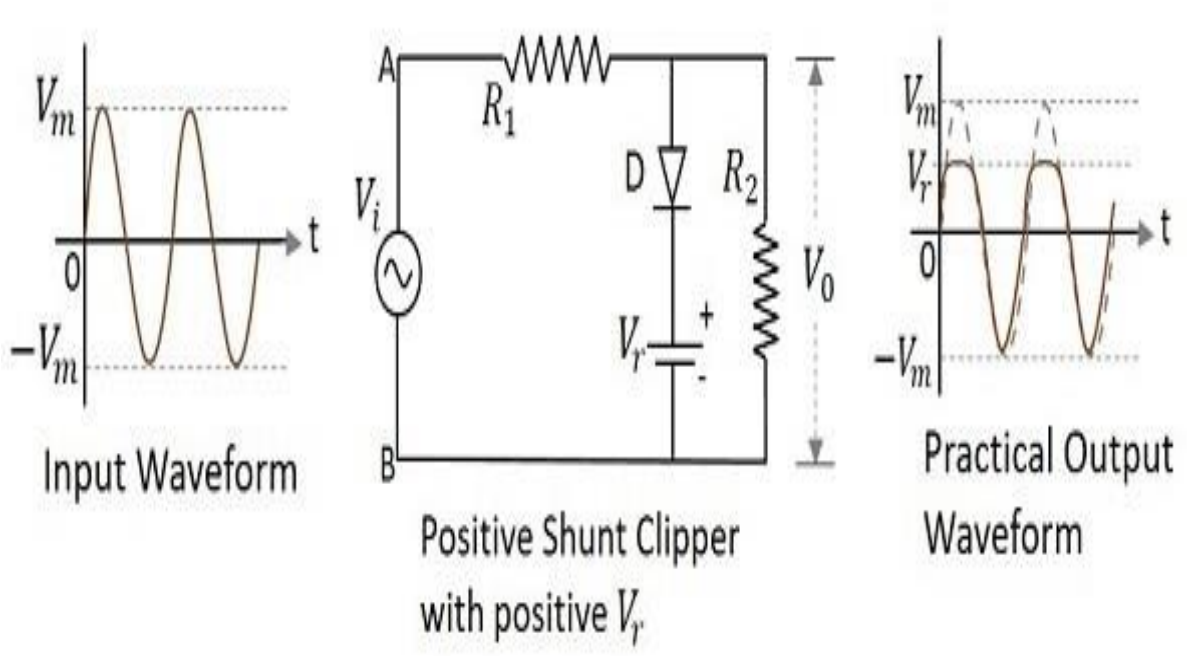
Positive Shunt Clipper

- A Clipper circuit in which the diode is connected in shunt to the input signal and that attenuates the positive portions of the waveform, is termed as **Positive Shunt Clipper**.



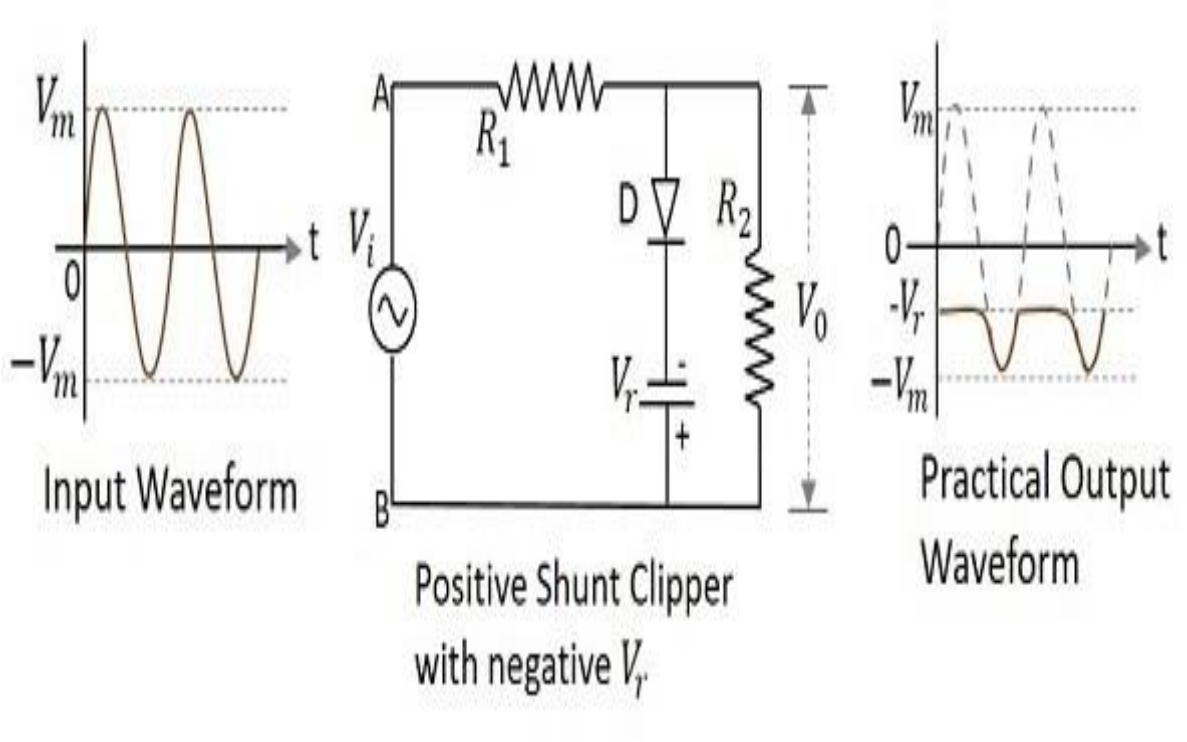
Positive Shunt Clipper with positive V_r

- A Clipper circuit in which the diode is connected in shunt to the input signal and biased with positive reference voltage V_r and that attenuates the positive portions of the waveform, is termed as **Positive Shunt Clipper with positive** V_r
- During the positive cycle of the input the diode gets forward biased and nothing but the reference voltage appears at the output.
- During its negative cycle, the diode gets reverse biased and behaves as an open switch. The whole of the input appears at the output.



Positive Shunt Clipper with negative V_r

- A Clipper circuit in which the diode is connected in shunt to the input signal and biased with negative reference voltage V_r and that attenuates the positive portions of the waveform, is termed as **Positive Shunt Clipper with negative** V_r
- During the positive cycle of the input, the diode gets forward biased and the reference voltage appears at the output. As the reference voltage is negative, the same voltage with constant amplitude is shown.
- During its negative cycle, the diode gets reverse biased and behaves as an open switch. Hence the input signal that is greater than the reference voltage, appears at the output.



Negative Clipper:

- The Clipper circuit that is intended to attenuate negative portions of the input signal can be termed as a **Negative Clipper**.

Among the negative diode clipper circuits, we have the following types.

- Negative Series Clipper

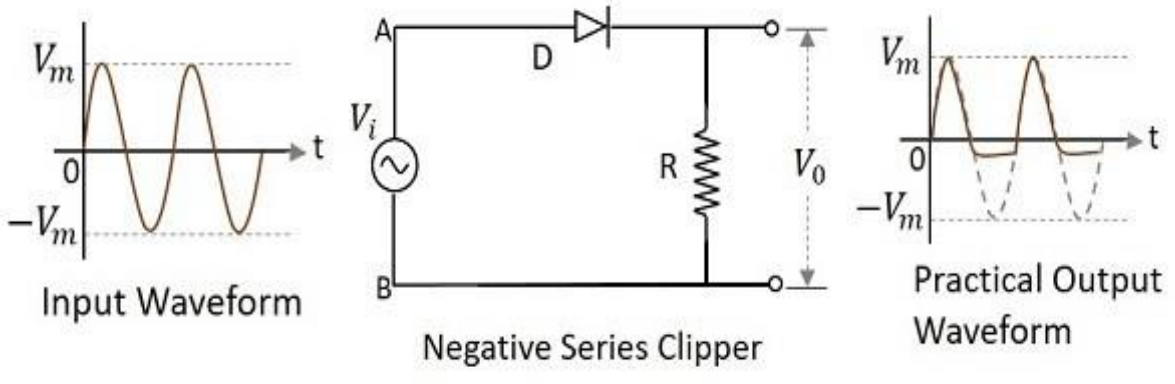
Negative Series Clipper with positive V_r
Negative Series Clipper with negative V_r

- Negative Shunt Clipper

Negative Shunt Clipper with positive V_r
Negative Shunt Clipper with negative V_r

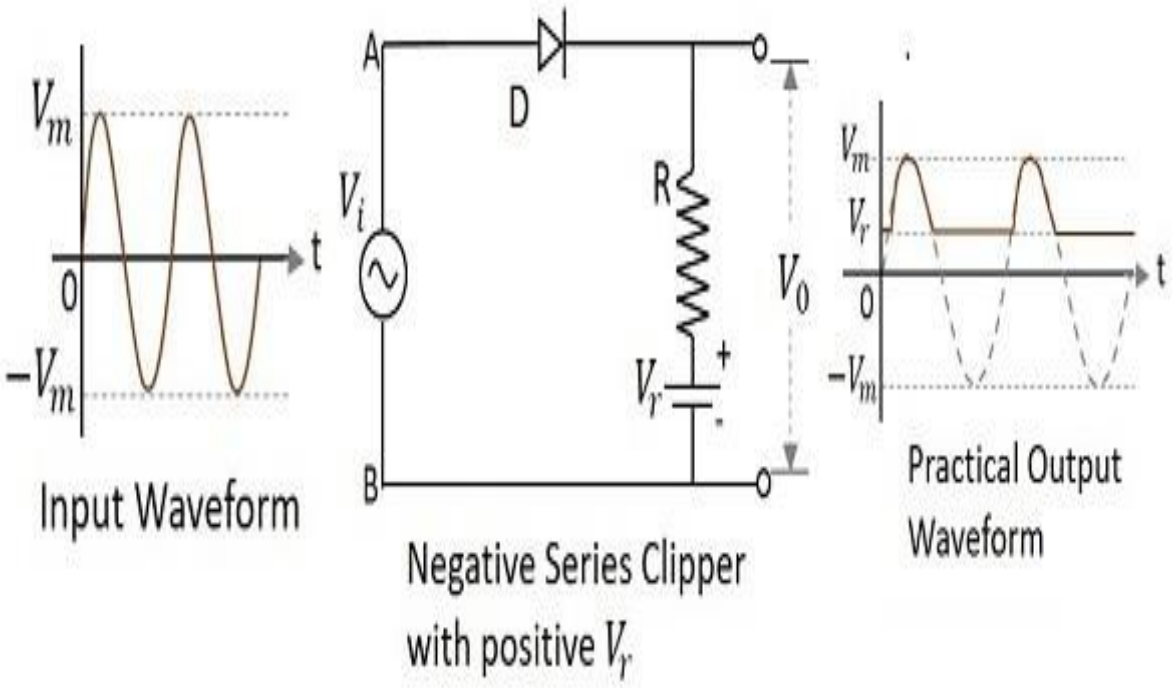
Negative Series Clipper

- A Clipper circuit in which the diode is connected in series to the input signal and that attenuates the negative portions of the waveform, is termed as **Negative Series Clipper**.



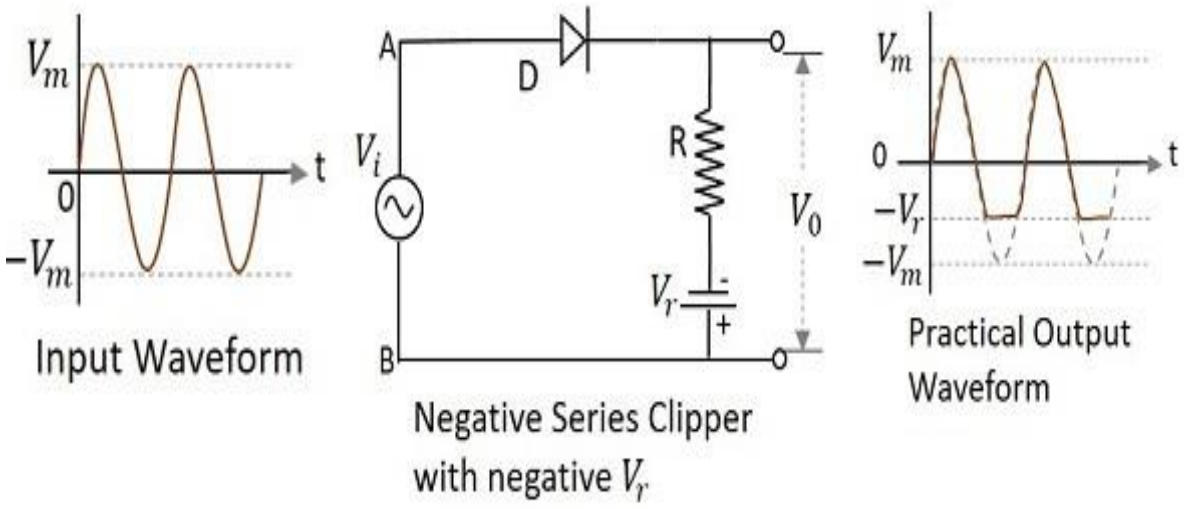
Negative Series Clipper with positive V_r

- A Clipper circuit in which the diode is connected in series to the input signal and biased with positive reference voltage V_r and that attenuates the negative portions of the waveform, is termed as **Negative Series Clipper with positive** V_r
- During the positive cycle of the input, the diode starts conducting only when the anode voltage value exceeds the cathode voltage value of the diode. As the cathode voltage equals the reference voltage applied, the output will be as shown.



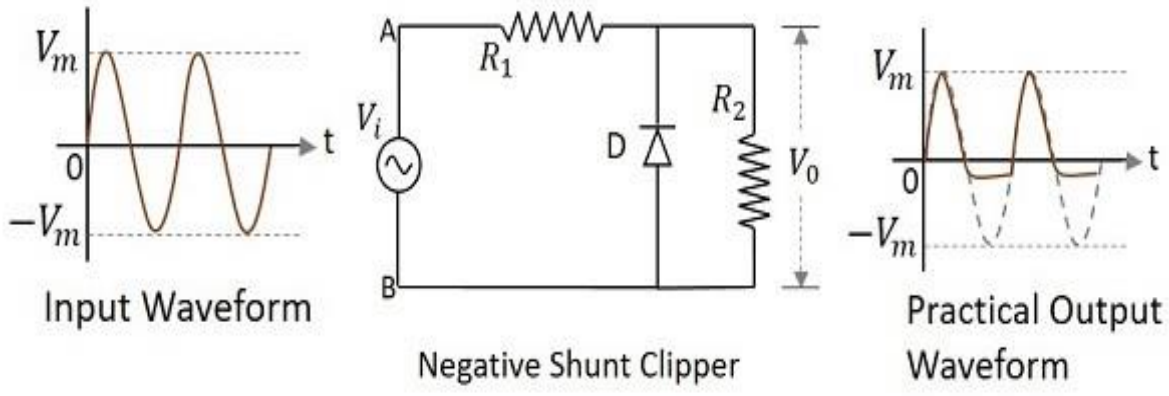
Negative Series Clipper with negative V_r

- A Clipper circuit in which the diode is connected in series to the input signal and biased with negative reference voltage $V_r$and that attenuates the negative portions of the waveform, is termed as **Negative Series Clipper with negative** V_r
- During the positive cycle of the input the diode gets forward biased and the input signal appears at the output.
- During its negative cycle, the diode gets reverse biased and hence will not conduct. But the negative reference voltage being applied, appears at the output. Hence the negative cycle of the output waveform gets clipped after this reference level.



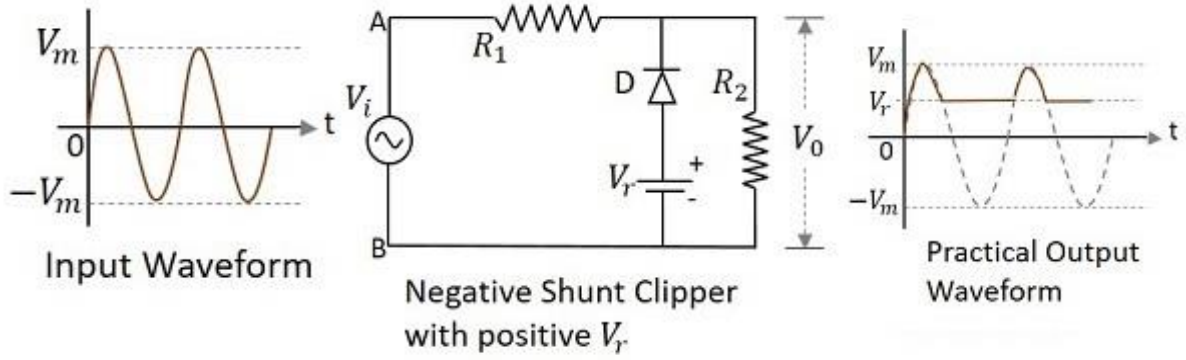
Negative Shunt Clipper:

- A Clipper circuit in which the diode is connected in shunt to the input signal and that attenuates the negative portions of the waveform, is termed as Negative Shunt Clipper.



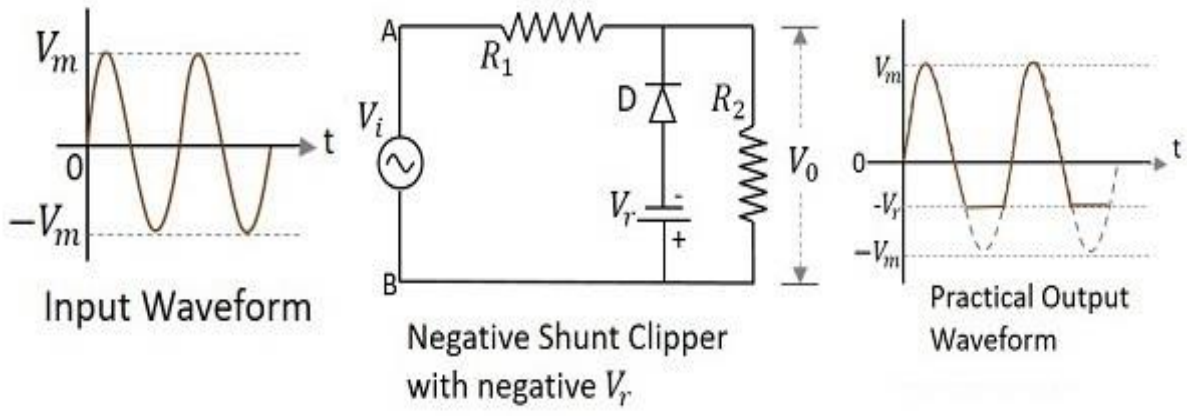
Negative Shunt Clipper with positive V_r

- A Clipper circuit in which the diode is connected in shunt to the input signal and biased with positive reference voltage **V_r** and that attenuates the negative portions of the waveform, is termed as **Negative Shunt Clipper with positive V_r**
- During the positive cycle of the input the diode gets reverse biased and behaves as an open switch. So whole of the input voltage, which is greater than the reference voltage applied, appears at the output. The signal below reference voltage level gets clipped off. During the negative half cycle, as the diode gets forward biased and the loop gets completed, no output is present.



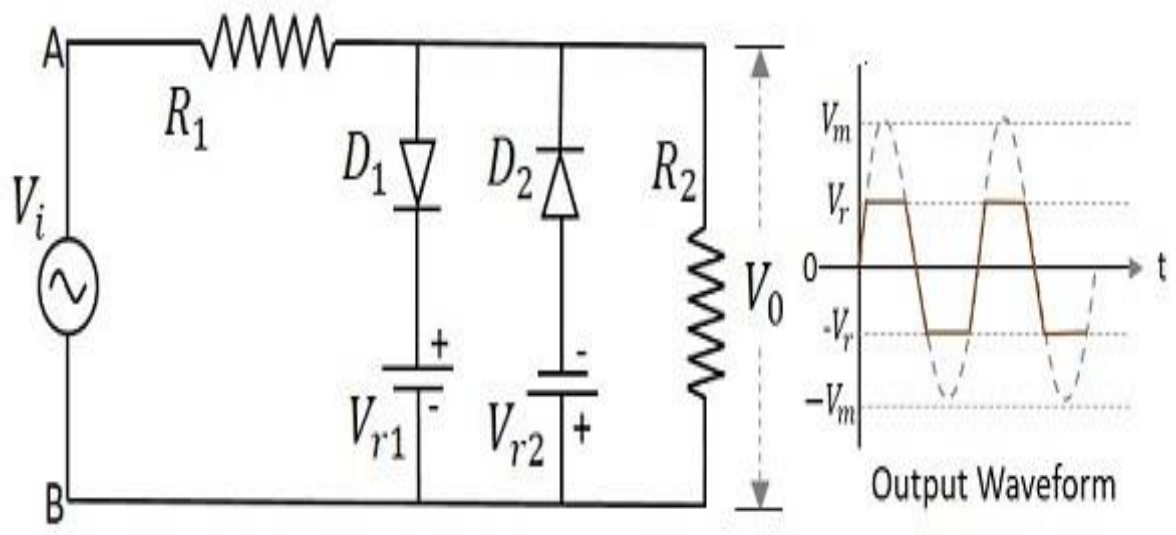
Negative Shunt Clipper with negative Vr

- A Clipper circuit in which the diode is connected in shunt to the input signal and biased with negative reference voltage **V_r** and that attenuates the negative portions of the waveform, is termed as **Negative Shunt Clipper with negative V_r**
- During the positive cycle of the input the diode gets reverse biased and behaves as an open switch. So whole of the input voltage, appears at the output V_o
- During the negative half cycle, the diode gets forward biased. The negative voltage up to the reference voltage, gets at the output and the remaining signal gets clipped off.



Two-way Clipper:

- This is a positive and negative clipper with a reference voltage V_r. The input voltage is clipped two-way both positive and negative portions of the input waveform with two reference voltages. For this, two diodes $D_1$and D_2 along with two reference voltages V_{r1} and V_{r2} are connected in the circuit.
- This circuit is also called as a **Combinational Clipper** circuit.



During the positive half of the input signal, the diode D_1 conducts making the reference voltage V_{r1} appear at the output. During the negative half of the input signal, the diode D_2 conducts making the reference voltage V_{r2} appear at the output. Hence both the diodes conduct alternatively to clip the output during both the cycles. The output is taken across the load resistor.

Applications:

- Used for the generation and shaping of waveforms
- Used for the protection of circuits from spikes
- Used for amplitude restorers
- Used as voltage limiters
- Used in television circuits
- Used in FM transmitters

MODELING AND ANALYSIS OF DIODE:

Equivalent Circuit:

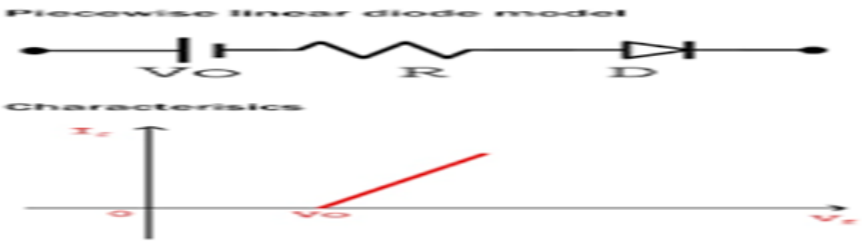
- An Equivalent circuit is a combination of elements properly chosen to best represent the actual characteristics of device in a particular operating region.
- Need of Equivalent circuit:
- To find the Parameters like current, voltage using circuit analysis methods.

Models:

- Piecewise linear model
- Assumptions : Linear even with small non linearity
- Constant voltage drop model
- Ideal diode model

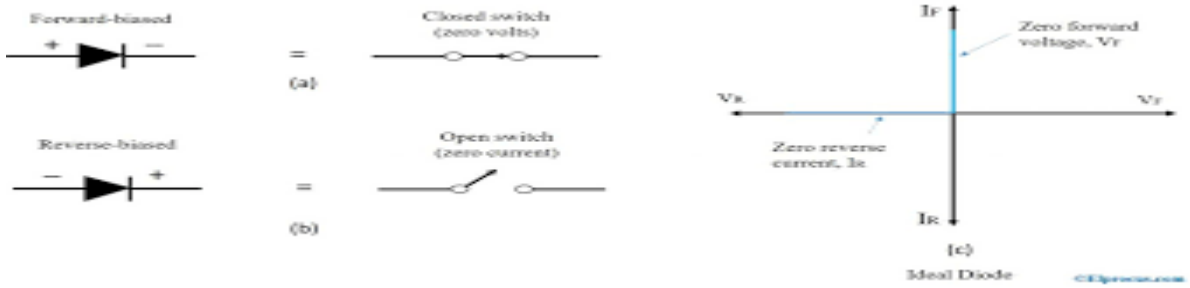
Piecewise linear model:

The real diode is modelled as 3 components in series: an ideal diode, a voltage source and a resistor



Ideal Diode Model:

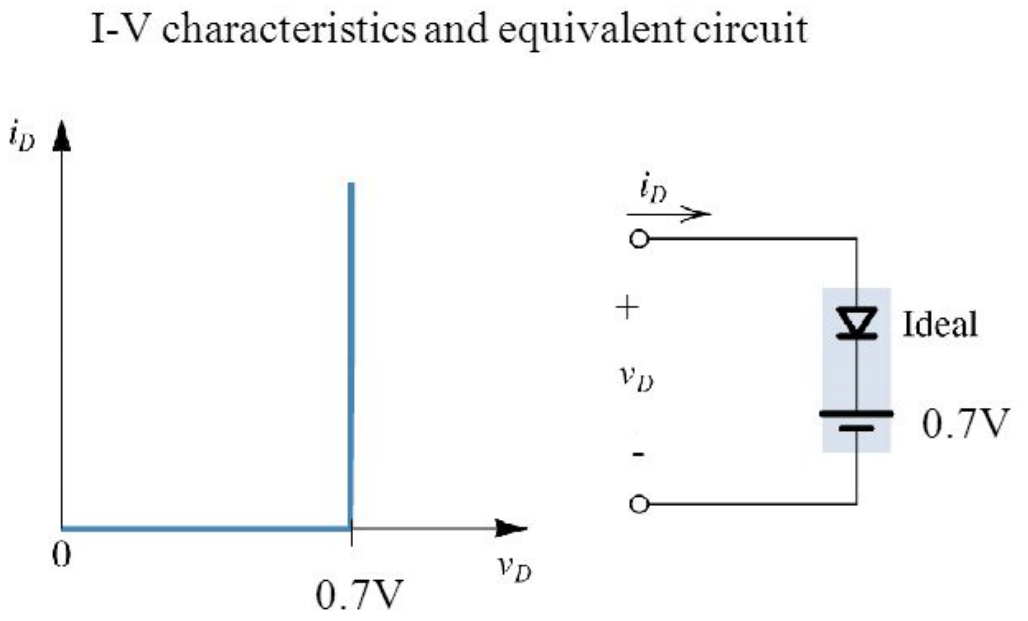
- a) The voltage across the diode is zero for forward bias.
- b) The slope of the current voltage curve is infinite for forward bias.
- c) The current across the diode is zero for reverse bias.



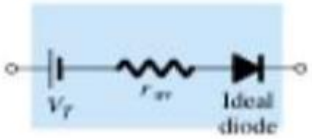
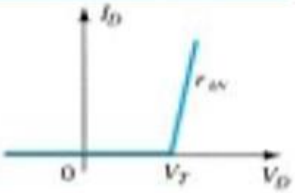
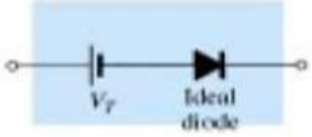
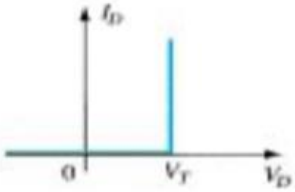
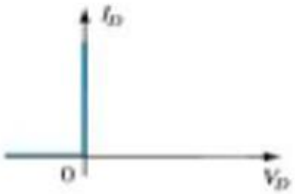
Constant Voltage Drop (CVD) Model:

- a) The voltage across the diode is a non-zero value for forward bias. Normally this is taken as 0.6 or 0.7 volts.
- b) The slope of the current voltage curve is infinite for forward bias.

c) The current across the diode is zero for reverse bias.



Diode Equivalent Circuits (Models)

Type	*Conditions*	*Model*	*Characteristics*
Piecewise-linear model			
Simplified model	$R_{network} \gg r_{av}$		
Ideal device	$R_{network} \gg r_{av}$ $E_{network} \gg V_T$		

TUTORIAL PROBLEMS:

1. The depletion region or space charge region or transition region in a semiconductor p-n junction diode has

a) electrons and holes.

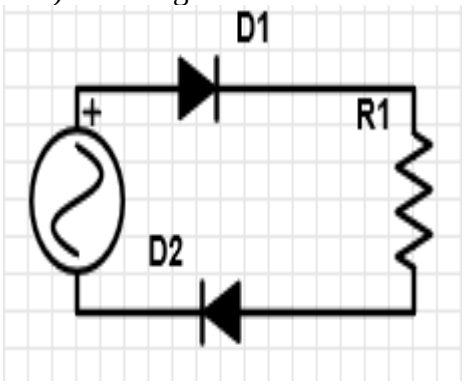
b) positive ions and electrons.

c) positive and negative ions.

d) negative ions and holes

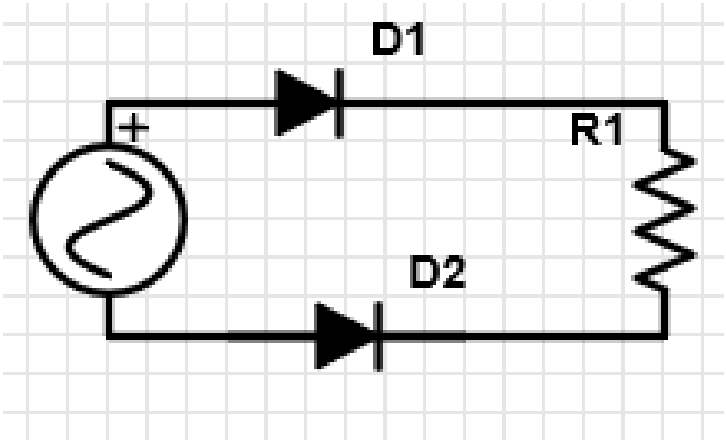
2. Which circuit has been represented in the associated circuit diagram?

a) Half wave rectifier
b) Full wave rectifier
c) NOT gate
d) AND gate



3. Which circuit has been represented in the associated circuit diagram?

a) Half wave rectifier
b) Full wave rectifier
c) NOT gate
d) AND gate

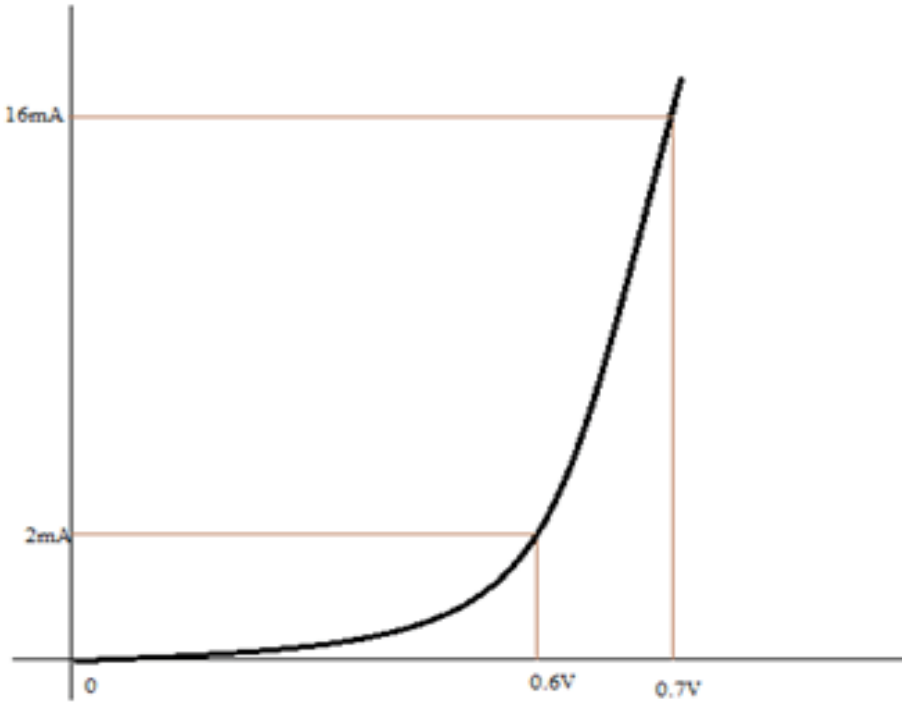


4. Which of the following is not a valid form of a diode equivalent circuit?
   a) Piecewise Linear Model

b) Ideal Diode Model
c) Simplified Model
d) Differential Model

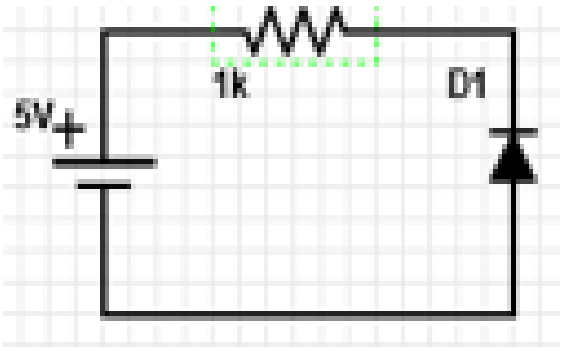
5. From the given I-V characteristics of a silicon diode, what is the approximate value of r_{av} between marked points?

a) 7 ohms
b) 11.2 ohms
c) 8 ohms
d) 6 ohms

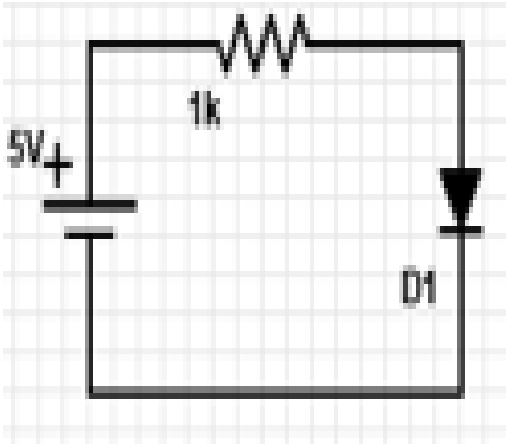


6. Assuming the diode in the given circuit diagram to be a silicon p-n junction diode, what is the current for the given circuit diagram?

a) 4.3 mA
b) 0
c) 43 mA
d) 5 mA



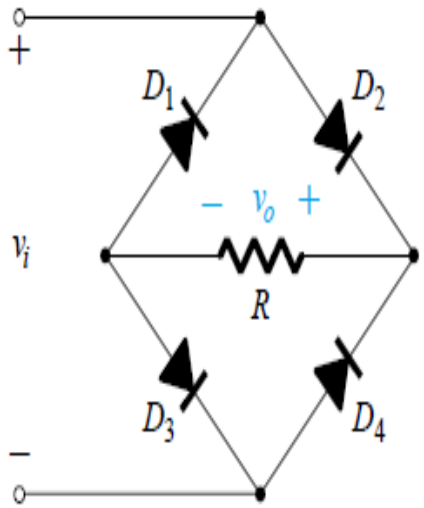
7. Assuming the diode in the given circuit diagram to be a silicon p-n junction diode, what is the current for the given circuit diagram?
   a) 0
   b) 5 mA
   c) 4.3 mA
   d) Can't be determined



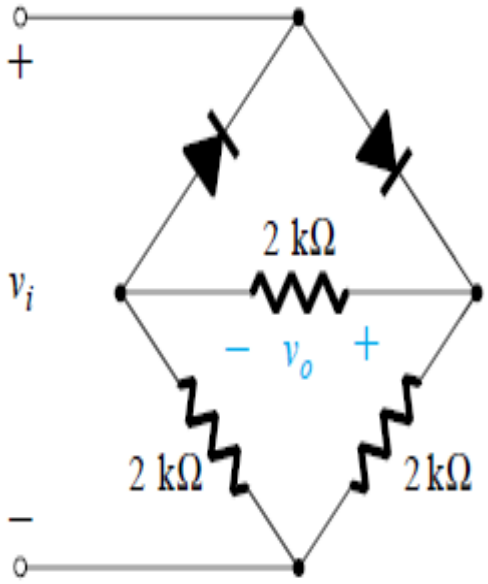
8. Which of the following equations is correct for a full wave rectified output?
   a) $|V_{dc}| = 0.318\ V_p$
   b) $|V_{dc}| = 0.636\ V_p$
   c) $|V_{dc}| = 0.477\ V_p$
   d) $|V_{dc}| = 0.211\ V_p$
9. Which of the following statements are true about the given circuit?

   a) The circuit is that of a bridge rectifier
   b) The PIV of the diode D1 must be greater than v0 for the circuit to function as a bridge rectifier
   c) For silicon diodes, the value of $v_0=(v_i-1.4)$ V

d) All of the mentioned



10. In the given circuit, what will be the nature of the output waveform?
    a) Half rectified
    b) Full rectified
    c) Sinusoidal
    d)DC



MODULE II
BJT AND AMPLIFIER CIRCUITS

Transistor

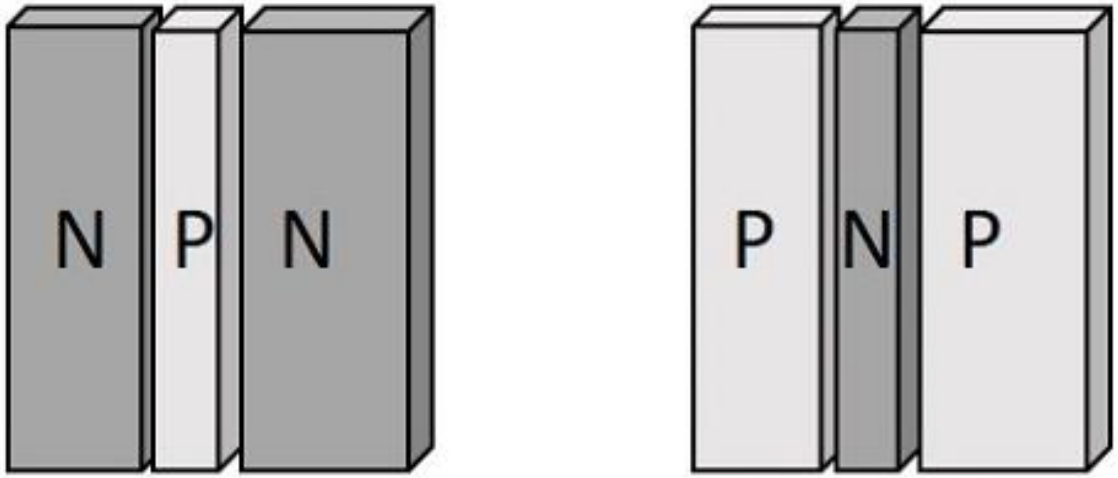
- A **Transistor** is a three terminal semiconductor device that regulates current or voltage flow and acts as a switch or gate for signals.
- If a P-type material or N-type material is added to a single PN junction, another junction will be formed. Such a formation is simply called as a **Transistor**.

Constructional Details of a Transistor

- The Transistor is a three terminal solid state device which is formed by connecting two diodes back to back. Hence it has got **two PN junctions**. Three terminals are drawn out of the three semiconductor materials present in it. This type of connection offers two types of transistors. They are **PNP** and **NPN** which means an N-type material between two Ptypes and the other is a P-type material between two N-types respectively.

Constructional Details of a Transistor

The three terminals drawn from the transistor indicate **Emitter, Base** and **Collector** terminals.



Emitter

- The left-hand side of the above shown structure can be understood as **Emitter**.
- This has a **moderate size** and is **heavily doped** as its main function is to **supply** a number of **majority carriers**, i.e. either electrons or holes.
- As this emits electrons, it is called as an Emitter.
- This is simply indicated with the letter **E**.

Base

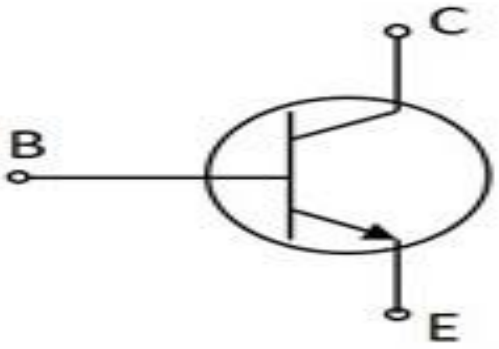
- The middle material in the above figure is the **Base**.
- This is **thin** and **lightly doped**.
- Its main function is to **pass** the majority carriers from the emitter to the collector.
- This is indicated by the letter **B**.

Collector

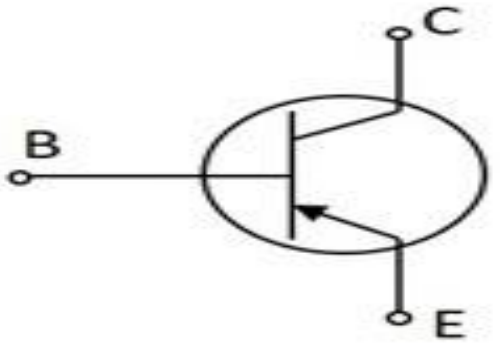
- The right side material in the above figure can be understood as a **Collector**.
- Its name implies its function of **collecting the carriers**.
- This is a **bit larger** in size than emitter and base. It is **moderately doped**.
- This is indicated by the letter **C**

Symbol

The **arrow-head** in the figures indicated the **emitter** of a transistor. As the collector of a transistor has to dissipate much greater power, it is made large. Due to the specific functions of emitter and collector, they are **not interchangeable**. Hence the terminals are always to be kept in mind while using a transistor.

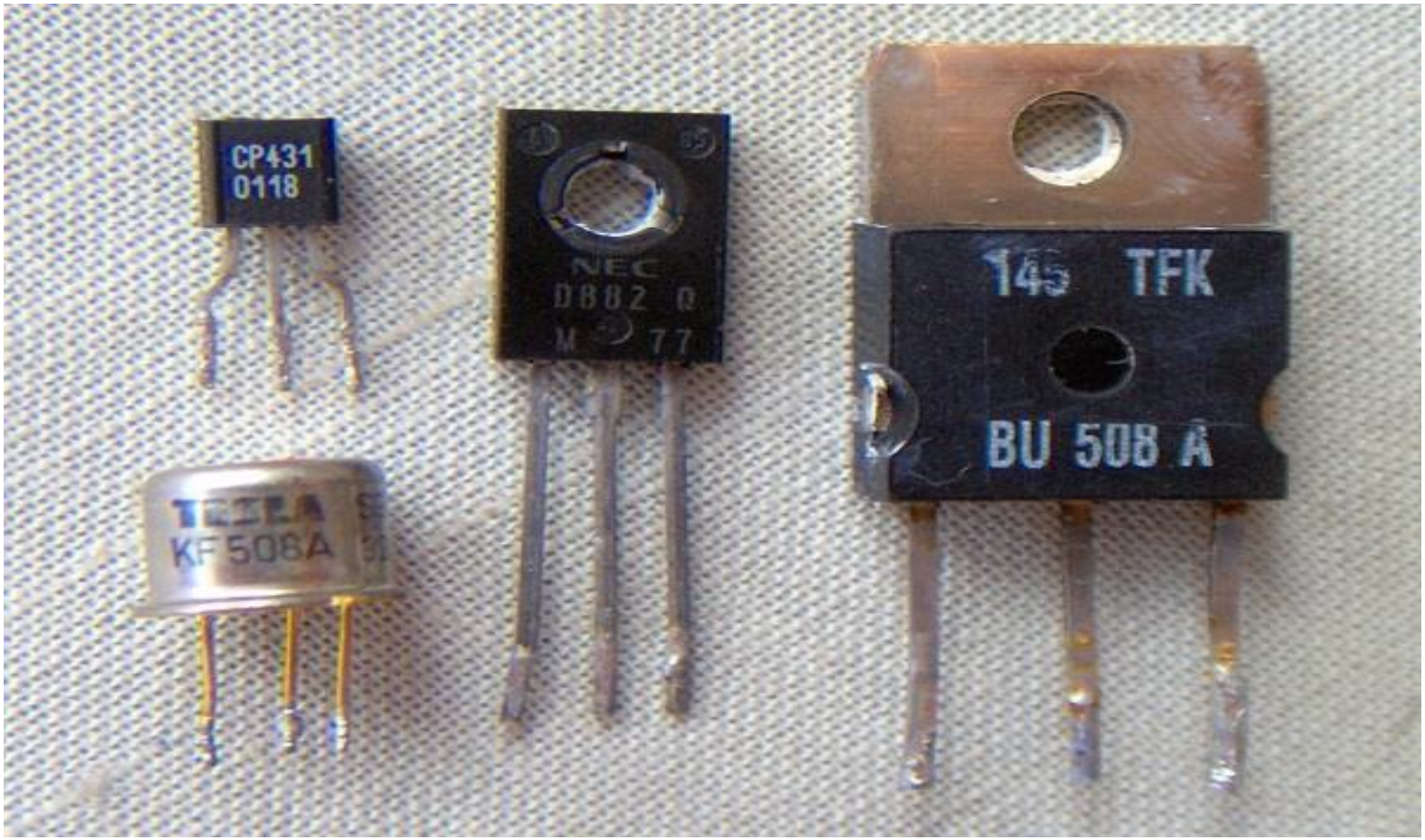


NPN transistor



PNP transistor

Transistor



Position of the terminals and symbol of BJT.

- Base is located at the middle and more thin from the level of collector and emitter
- The emitter and collector terminals are made of the same type of semiconductor material, while the base of the other type of material

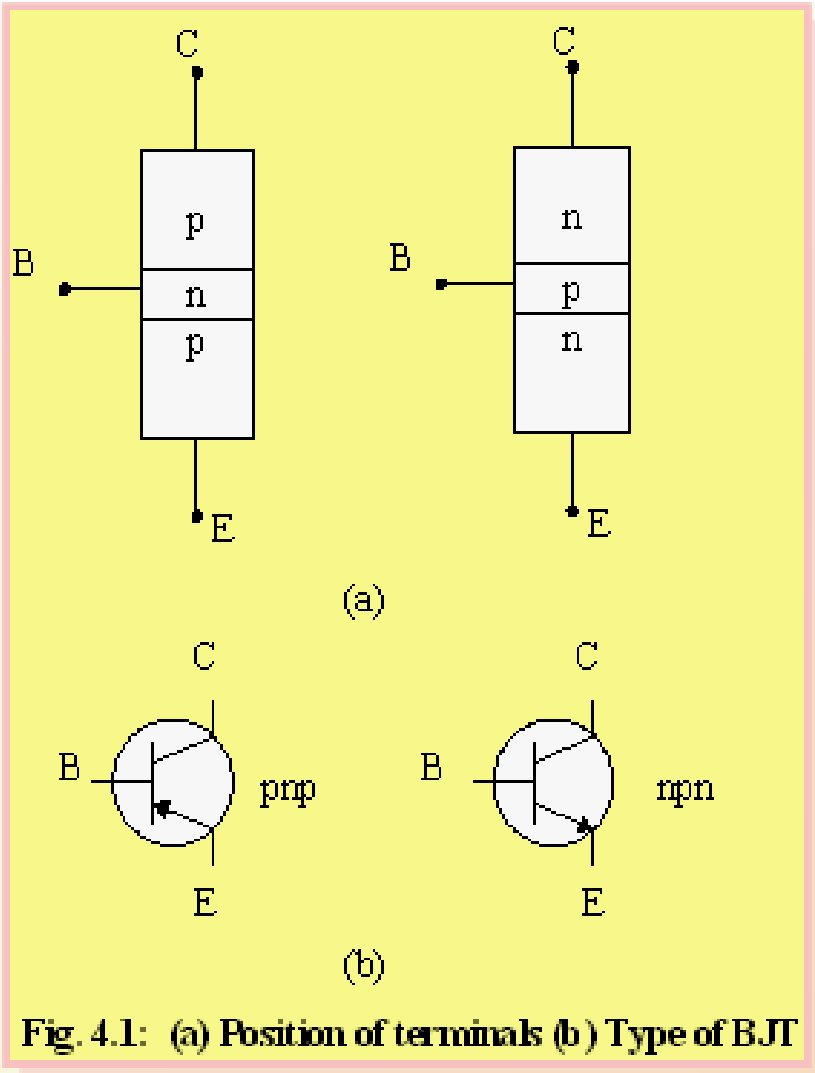
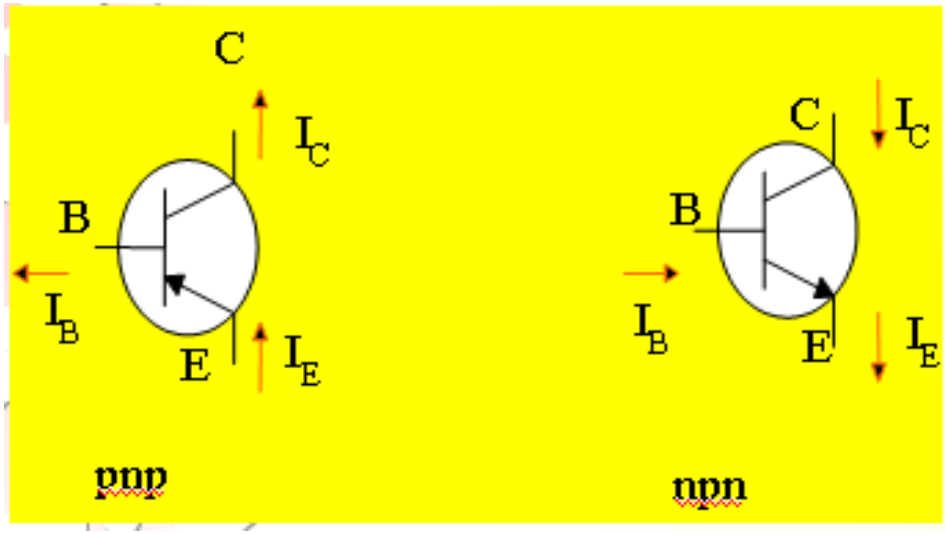


Fig. 4.1: (a) Position of terminals (b) Type of BJT

Transistor currents



I_C=the collector current
I_B= the base current
I_E= the emitter current

-The arrow is always drawn on the emitter

-The arrow always point toward the n-type

-The arrow indicates the direction of the emitter current:

pnp:E→ B
npn: B→ E

- By imaging the analogy of diode, transistor can be construct like two diodes that connetecd together.
- It can be conclude that the work of transistor is base on work of diode.

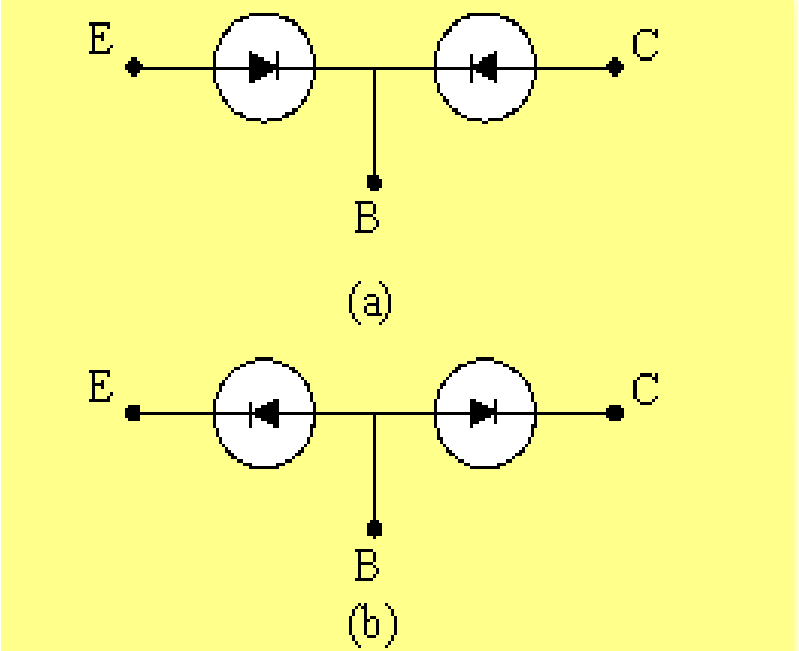


Fig. 4.2: (a) pnp transistor (b) npn transistor

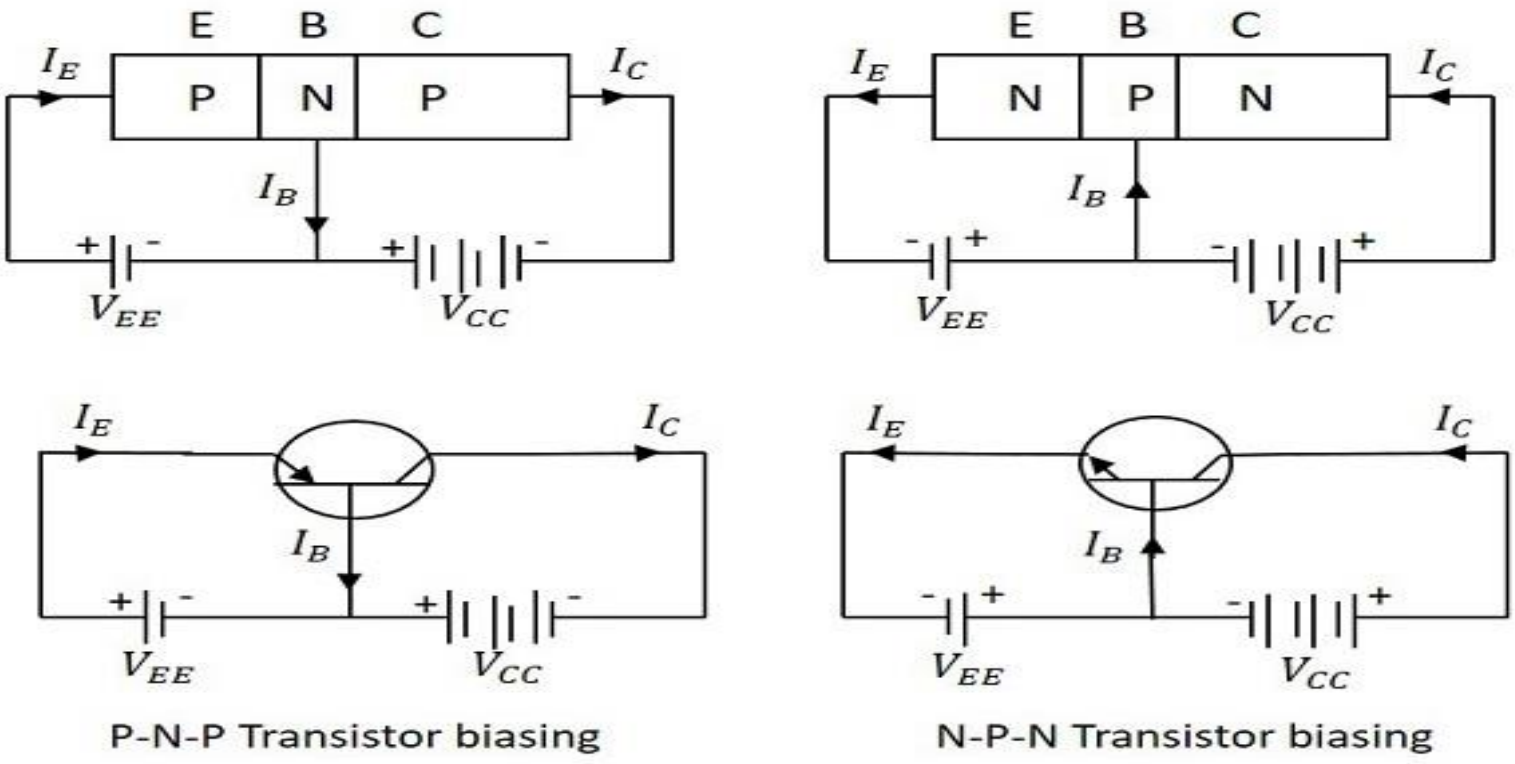
Transistor Biasing

- **Biasing** is controlling the operation of the circuit by providing power supply. The function of both the PN junctions is controlled by providing bias to the circuit through some dc supply.
- we have two junctions here. As one junction is between the emitter and base, that is called as **Emitter-Base junction** and likewise, the other is **Collector-Base junction**.

Transistor Biasing

- The N-type material is provided negative supply and P-type material is given positive supply to make the circuit **Forward bias**.
- The N-type material is provided positive supply and P-type material is given negative supply to make the circuit **Reverse bias**.
- By applying the power, the **emitter base junction** is always **forward biased** as the emitter resistance is very small. The **collector base junction** is **reverse biased** and its resistance is a bit higher. A small forward bias is sufficient at the emitter junction whereas a high reverse bias has to be applied at the collector junction.

Transistor Biasing



P-N-P Transistor biasing

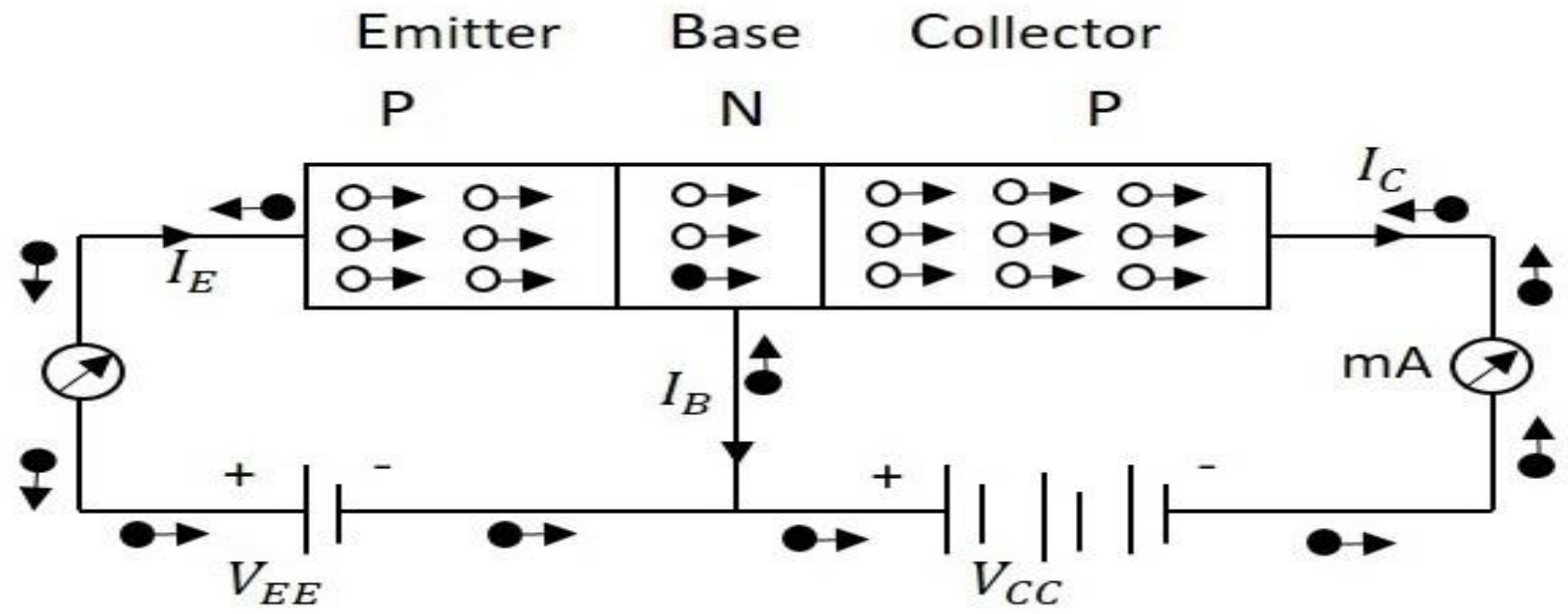
N-P-N Transistor biasing

The direction of current indicated in the circuits above, also called as the **Conventional Current**, is the movement of hole current which is **opposite to the electron current**.

Operation of PNP Transistor

- The voltage $\mathbf{V_{EE}}$ provides a positive potential at the emitter which repels the holes in the P-type material and these holes cross the emitter-base junction, to reach the base region. There a very low percent of holes re-combine with free electrons of N-region. This provides very low current which constitutes the base current $\mathbf{I_B}$. The remaining holes cross the collector-base junction, to constitute collector current $\mathbf{I_C}$, which is the hole current.
- As a hole reaches the collector terminal, an electron from the battery negative terminal fills the space in the collector. This flow slowly increases and the electron minority current flows through the emitter, where each electron entering the positive terminal of $\mathbf{V_{EE}}$, is replaced by a hole by moving towards the emitter junction. This constitutes emitter current $\mathbf{I_E}$.

Operation of PNP Transistor

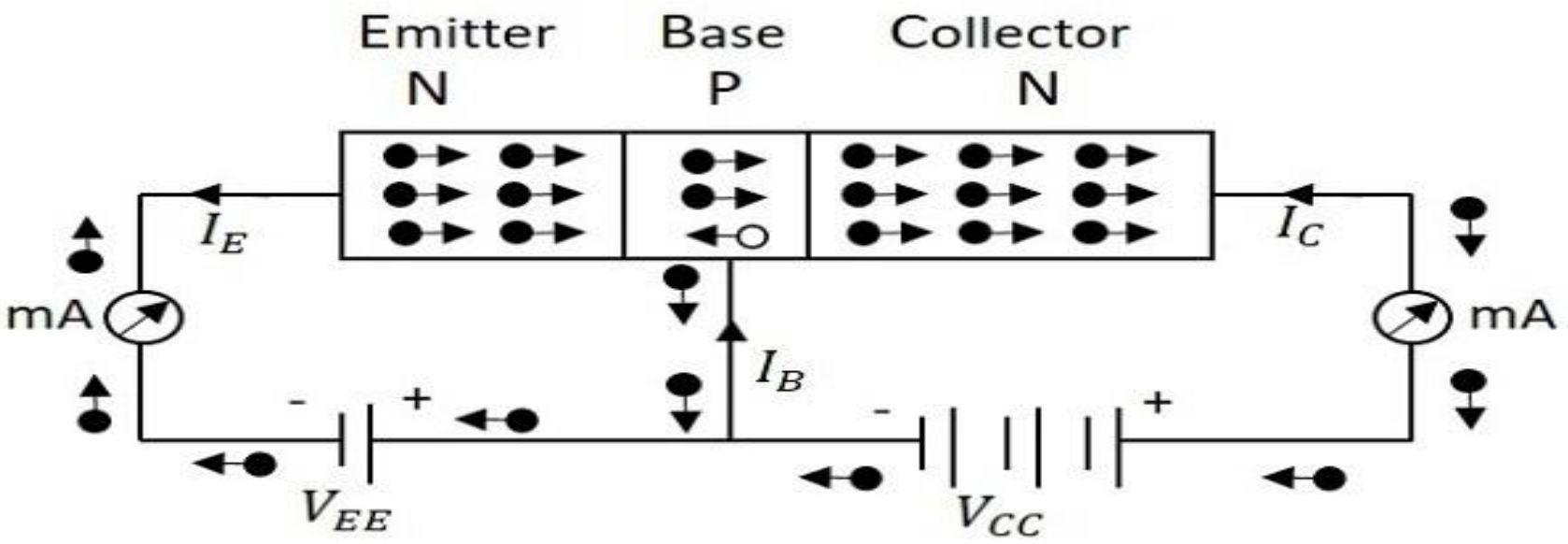


The conduction in a PNP transistor takes place through holes.
The collector current is slightly less than the emitter current.
The increase or decrease in the emitter current affects the collector current.

Operation of NPN Transistor

- The voltage $\mathbf{V_{EE}}$ provides a negative potential at the emitter which repels the electrons in the N-type material and these electrons cross the emitter-base junction, to reach the base region. There, a very low percent of electrons re-combine with free holes of P-region. This provides very low current which constitutes the base current $\mathbf{I_B}$. The remaining holes cross the collector-base junction, to constitute the collector current $\mathbf{I_C}$.
- As an electron reaches out of the collector terminal, and enters the positive terminal of the battery, an electron from the negative terminal of the battery $\mathbf{V_{EE}}$ enters the emitter region. This flow slowly increases and the electron current flows through the transistor.

Operation of NPN Transistor



The conduction in a NPN transistor takes place through electrons.

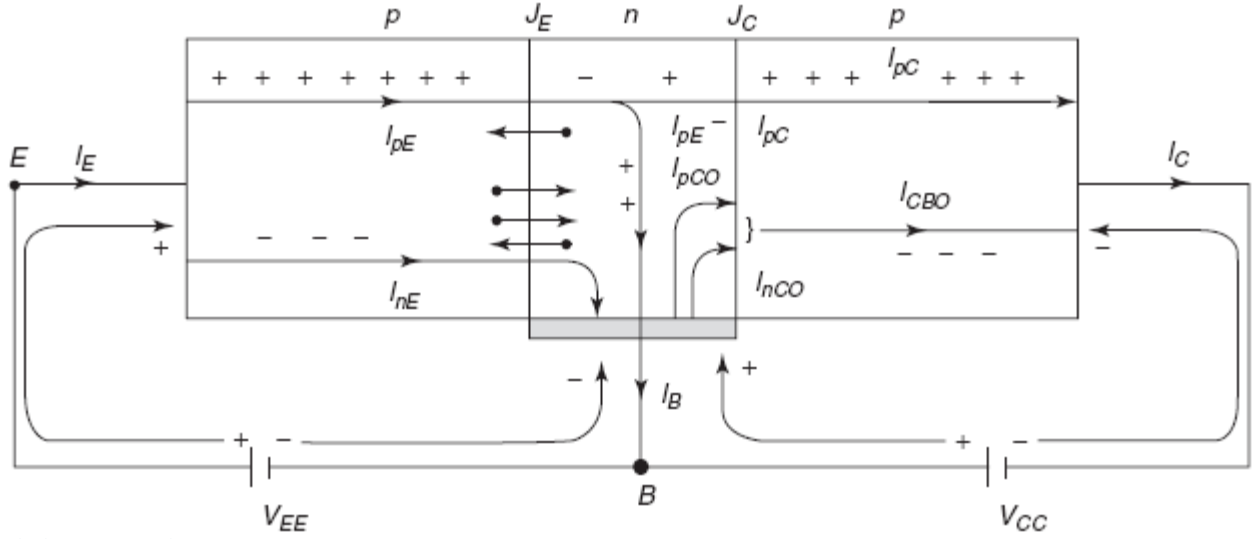
The collector current is higher than the emitter current.

The increase or decrease in the emitter current affects the collector current.

TRANSISTOR CURRENT COMPONENTS

❖ **Current Components in *p–n–p Transistor***

- Both biasing potentials have been applied to a *p–n–p transistor,* with the resulting majority and minority carrier flow indicated.
- The width of the depletion region clearly indicates which junction is forward-biased and which is reverse-biased.
- The magnitude of the base current is typically in the order of microamperes as compared to mill amperes for the emitter and collector currents. The large number of these majority carriers will diffuse across the reverse-biased junction into the *p-type material connected to* the collector terminal



Direction of flow of current in *p–n–p transistor with the base–emitter junction forward-biased* and the collector–base junction reverse-biased

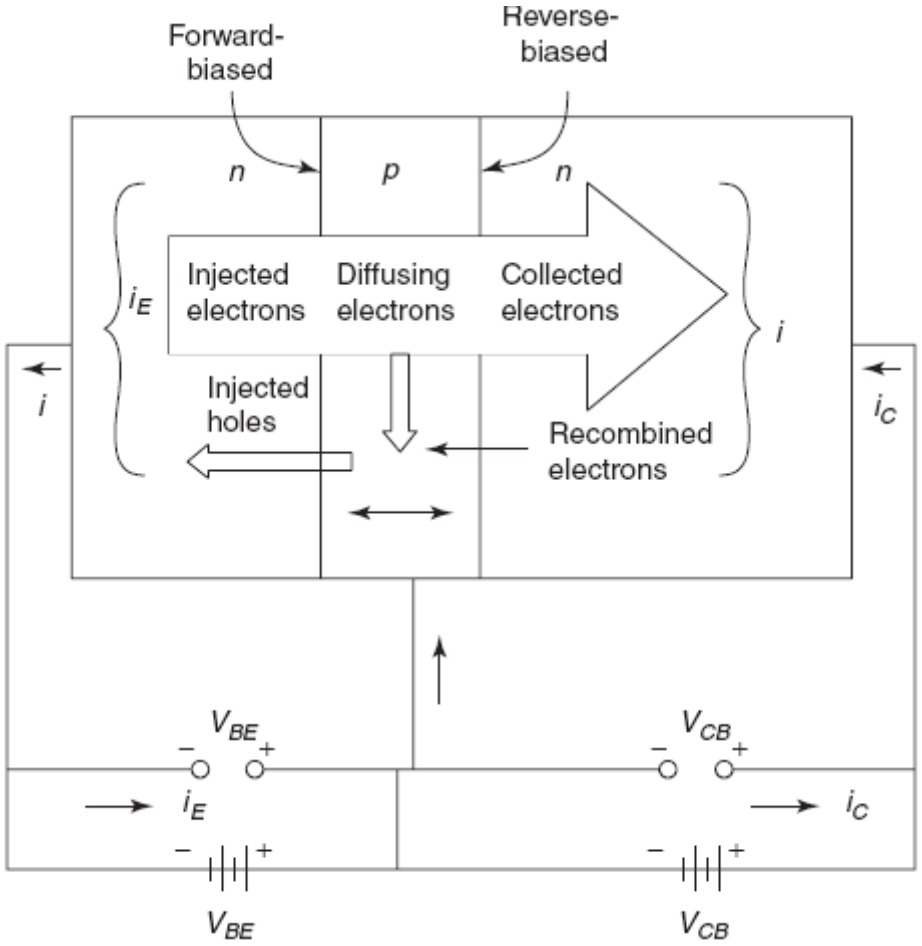
TRANSISTOR CURRENT COMPONENTS

❖ **Current Components in an *n–p–n Transistor***

➢ The operation of an *n–p–n transistor is the same as that of a p–n–p transistor, but with the roles played by* the electrons and holes interchanged.

➢ The polarities of the batteries and also the directions of various currents are to be reversed.

➢ Here the majority electrons from the emitter are injected into the base and the majority holes from the base are injected into the emitter region. These two constitute the emitter current.



The majority and the minority carrier current flow in a forward-biased *n–p–n transistor*

Advantages

- High voltage gain.
- Lower supply voltage is sufficient.
- Most suitable for low power applications.
- Smaller and lighter in weight.
- Mechanically stronger than vacuum tubes.
- No external heating required like vacuum tubes.
- Very suitable to integrate with resistors and diodes to produce ICs.

Disadvantages

- They cannot be used for high power applications due to lower power dissipation.
- They have lower input impedance and they are temperature dependent.

Transistor Configurations

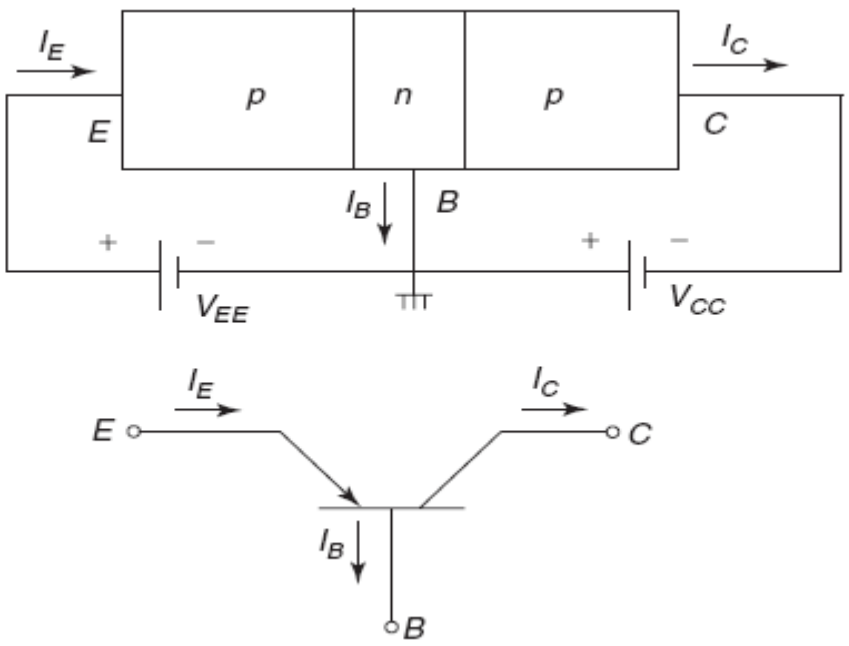
- Any transistor has three terminals, the **emitter**, the **base**, and the **collector**. Using these 3 terminals the transistor can be connected in a circuit with one terminal common to both input and output in three different possible configurations.
- The three types of configurations are **Common Base, Common Emitter** and **Common Collector** configurations. In every configuration, the emitter junction is forward biased and the collector junction is reverse biased.

CB, CE AND CC CONFIGURATIONS

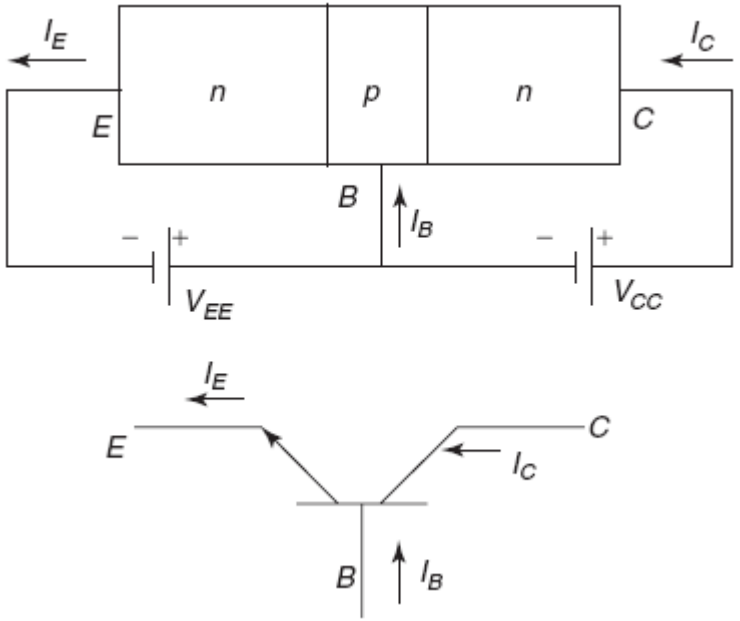
❖ Depending on the common terminal between the input and the output circuits of a transistor, it may be operated in the common-base mode, or the common-emitter mode, or the common-collector mode.

❖ **Common-base (CB) Mode**

➢ In this mode, the base terminal is common to both the input and the output circuits. This mode is also referred to as the ground–base configuration.



Notation and symbols used for the common-base configuration of a *p–n–p transistor*

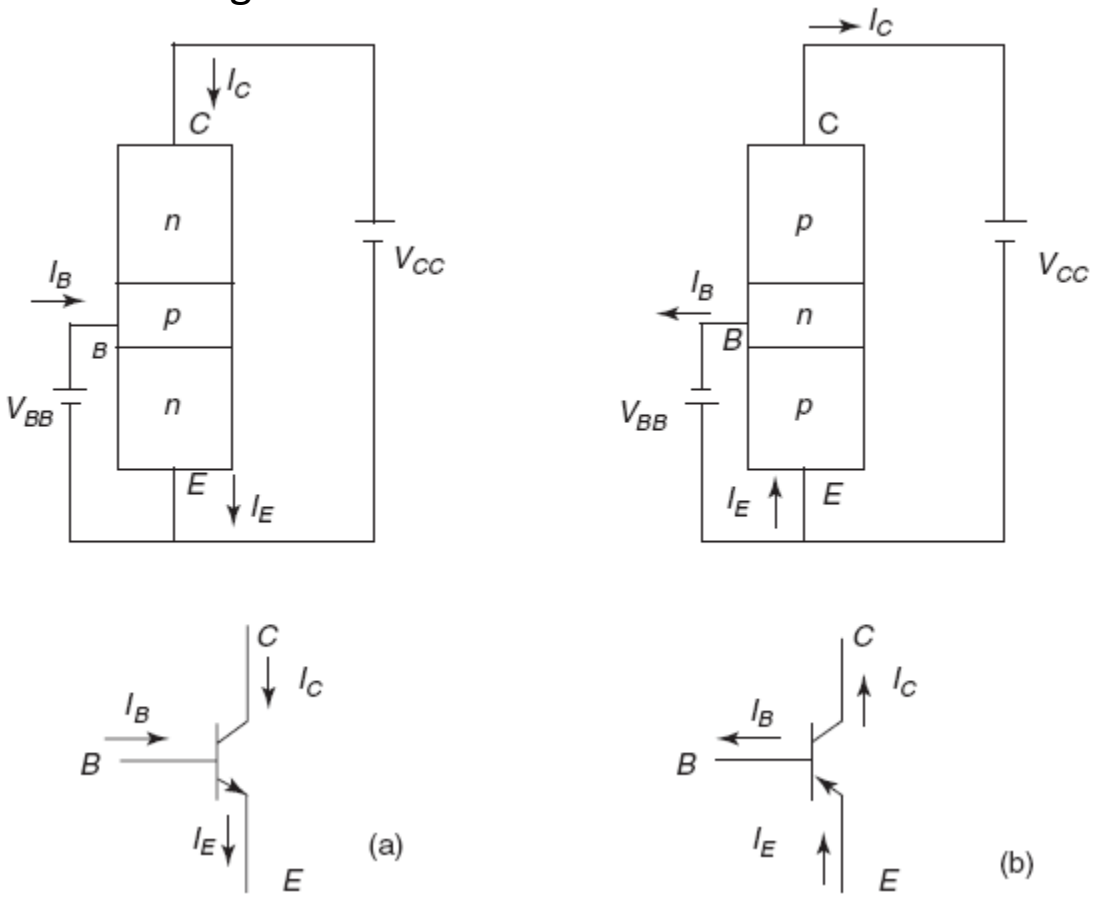


Common-base configuration of an *n–p–n transistor*

CB, CE AND CC CONFIGURATIONS

❖ Common-emitter (CE) Mode

➢ When the emitter terminal is common to both the input and the output circuits, the mode of operation is called the common-emitter (CE) mode or the ground–emitter configuration of the transistor.

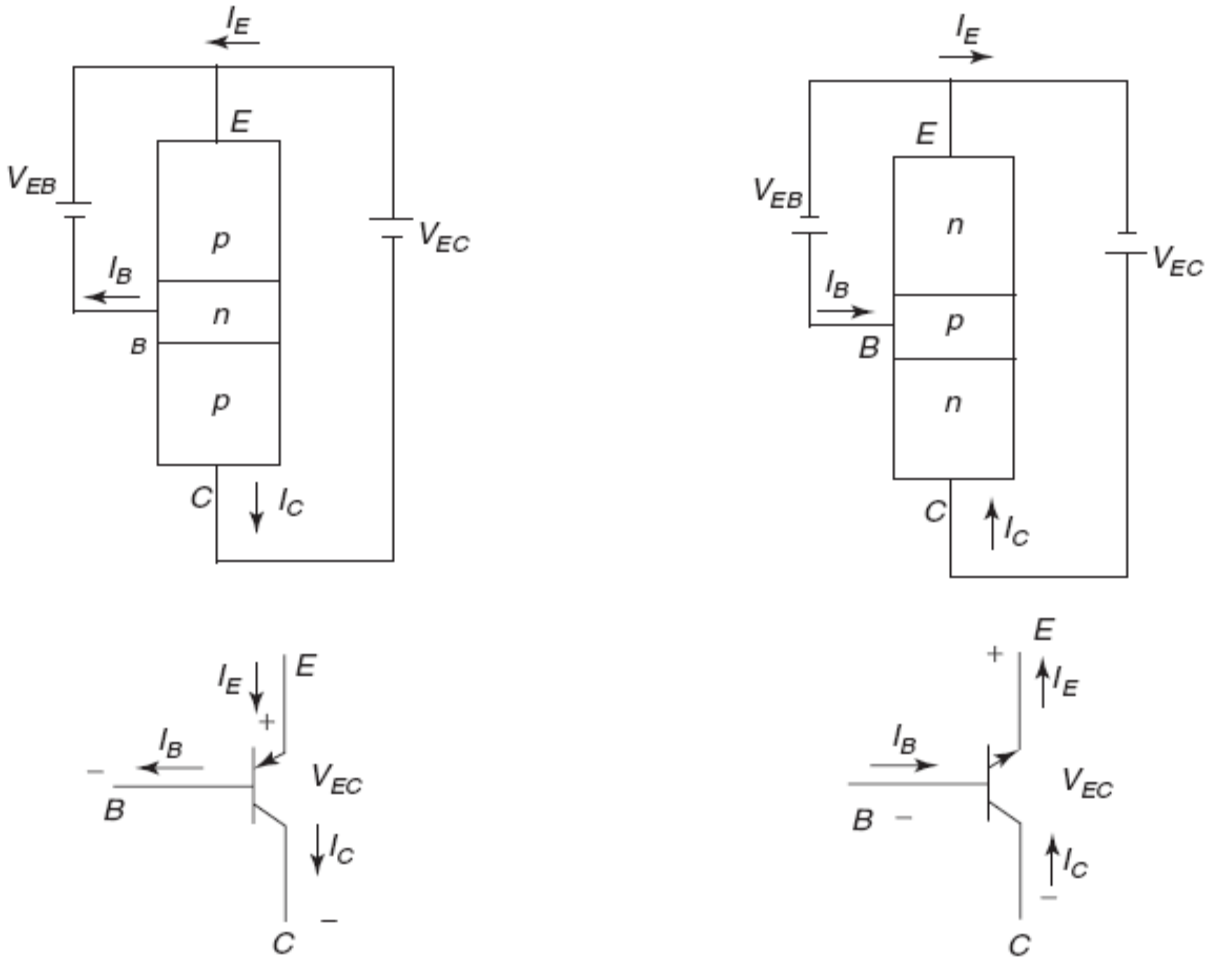


Notation and symbols for common-emitter configuration (a) *n–p–n transistor (b) p–n–p transistor*

CB, CE AND CC CONFIGURATIONS

❖ Common-collector (CC) Mode

➢ When the collector terminal of the transistor is common to both the input and the output terminals, the mode of operation is known as the common-collector (CC) mode or the ground–collector configuration.



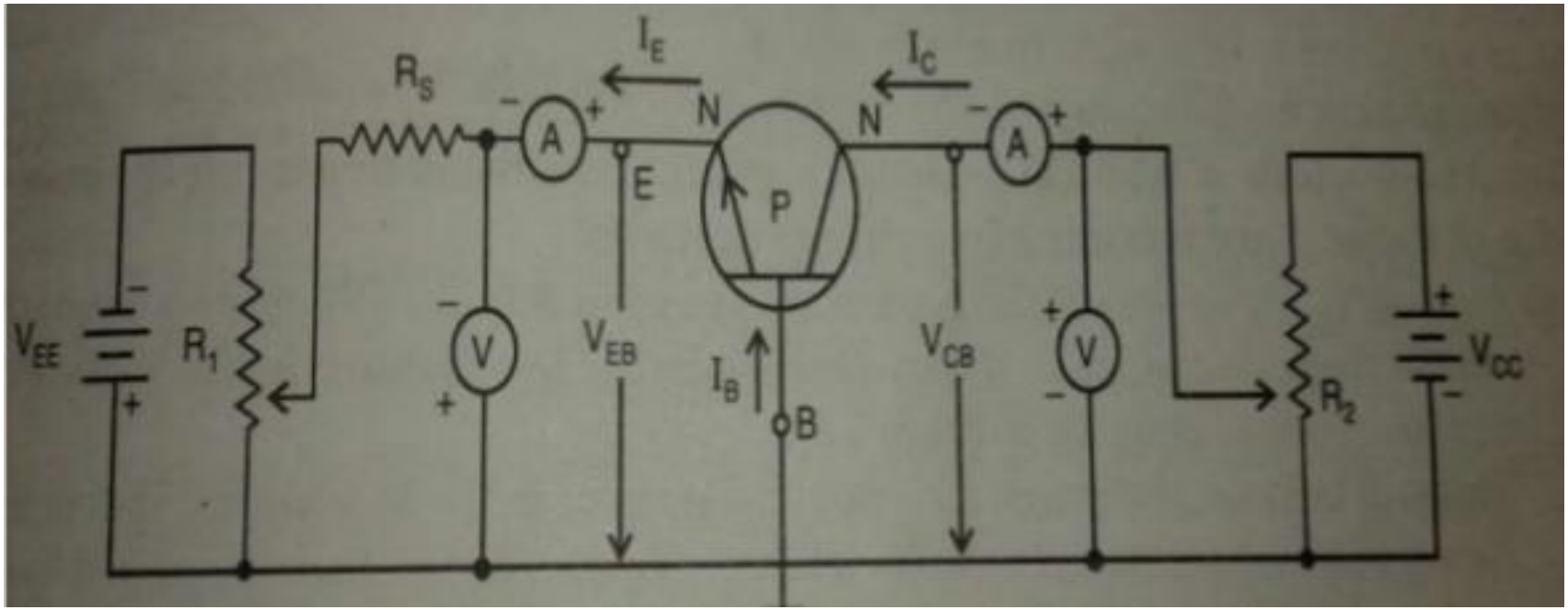
Common-collector configuration

Transistor Characteristics

- **Input Characteristics**: These describe the changes in input current with the variation in the values of input voltage keeping the output voltage constant.
- **Output Characteristics**: This is a plot of output current versus output voltage with constant input current.
- **Current Transfer Characteristics**: This characteristic curve shows the variation of output current in accordance with the input current, keeping output voltage constant.

Common Base (CB) Configuration

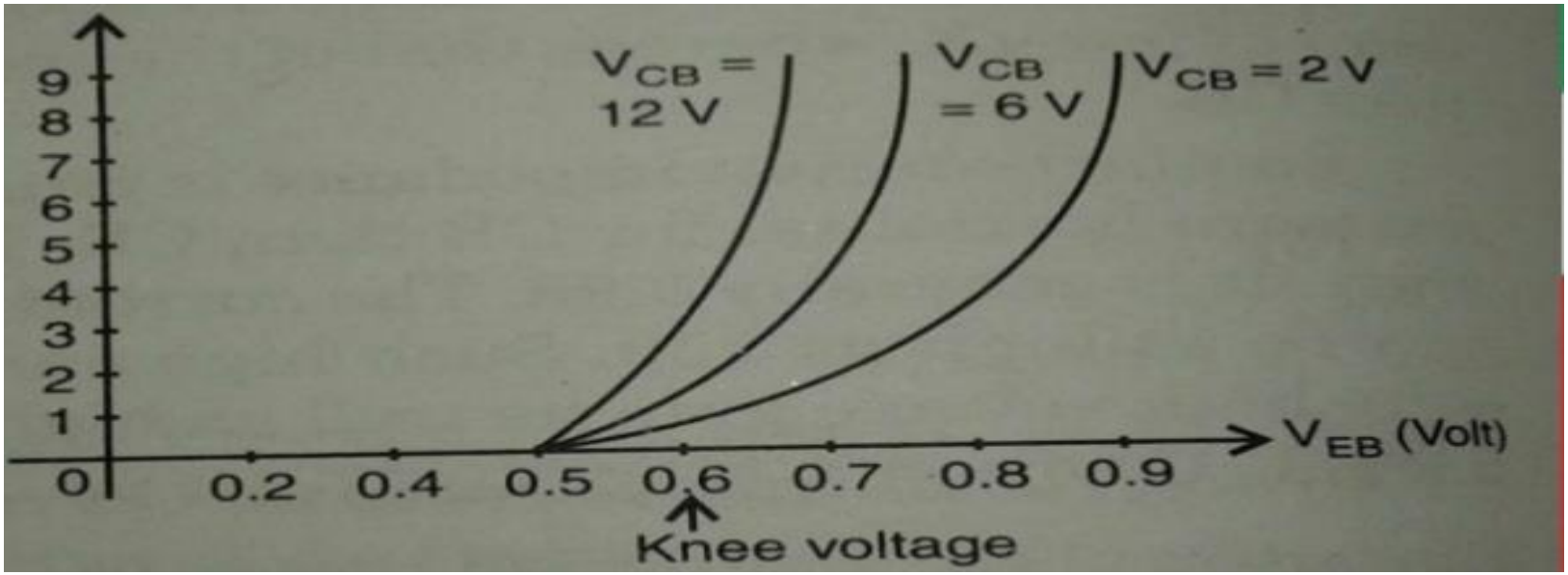
The name itself implies that the **Base** terminal is taken as common terminal for both input and output of the transistor.



Input or driving point characteristics.

- The input characteristics of a CB configuration circuit which describes the variation of emitter current, I_E with Base-Emitter voltage, V_{BE} keeping Collector-Base voltage, V_{CB} constant.

Input or driving point characteristics.

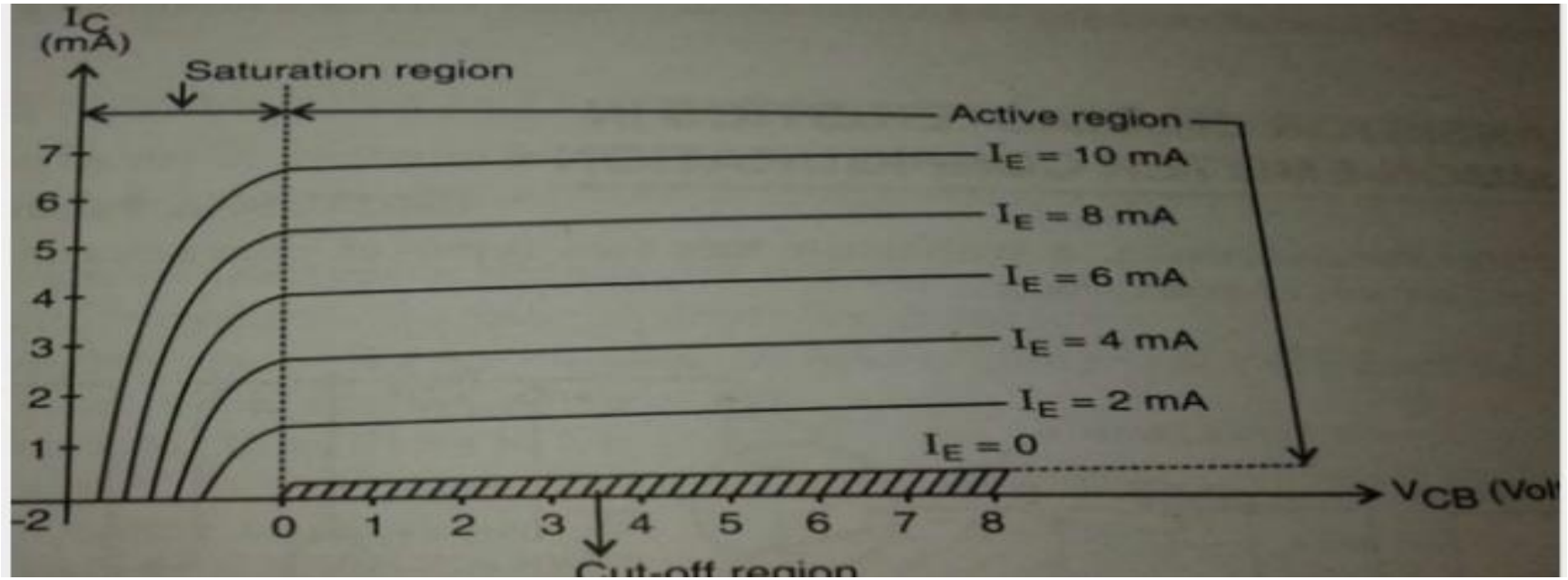


This leads to the expression for the input resistance as

$$R_{in} = \left.\frac{\Delta V_{BE}}{\Delta I_E}\right|_{V_{CB}=constant}$$

Output or collector characteristics

The output characteristics of CB configuration (Figure 3) show the variation of collector current, I_C with V_{CB} when the emitter current, I_E is held constant.



Output or collector characteristics

- The output characteristics has 3 basic regions:
  - Active region –defined by the biasing arrangements
  - Cutoff region – region where the collector current is 0A
  - Saturation region- region of the characteristics to the left of V_{CB} = 0V
- From the graph shown, the output resistance can be obtained as:

$$R_{out} = \left.\frac{\Delta V_{CB}}{\Delta I_C}\right|_{I_E=constant}$$

Active region	Saturation region	Cut-off region
• I_E increased, Ic increased • BE junction forward bias and CB junction reverse bias • Refer to the graf, $Ic \approx I_E$ • Ic not depends on V_{CB} • Suitable region for the transistor working as amplifier	• BE and CB junction is forward bias • Small changes in V_{CB} will cause big different to Ic • The allocation for this region is to the left of V_{CB}= 0 V.	• Region below the line of I_E=0 A • BE and CB is reverse bias • no current flow at collector, only leakage current

Current Transfer Characteristics

- The current transfer characteristics for CB configuration which illustrates the variation of I_C with the I_E keeping V_{CB} as a constant. The resulting current gain has a value less than 1 and can be mathematically expressed as:

$$\alpha = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=constant}$$

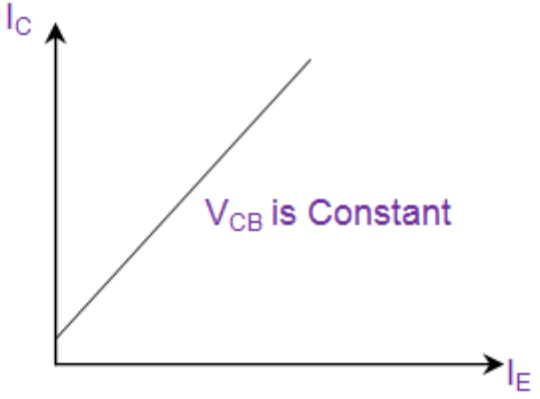


Figure 4 Current Transfer Characteristics for CB Configuration

Characteristics of CB configuration

- This configuration provides voltage gain but no current gain.
- Being V_{CB} constant, with a small increase in the Emitter-base voltage V_{EB}, Emitter current I_E gets increased.
- Emitter Current I_E is independent of Collector voltage V_{CB}.
- Collector Voltage V_{CB} can affect the collector current I_C only at low voltages, when V_{EB} is kept constant.
- The input resistance $\mathbf{R_i}$ is the ratio of change in emitter-base voltage (ΔV_{EB}) to the change in emitter current (ΔI_E) at constant collector base voltage V_{CB}.

$$R_i = \frac{\Delta V_{EB}}{\Delta I_E} \quad \text{at constant } V_{CB}$$

- As the input resistance is of very low value, a small value of V_{EB} is enough to produce a large current flow of emitter current I_E.
- The output resistance $\mathbf{R_o}$ is the ratio of change in the collector base voltage (ΔV_{CB}) to the change in collector current (ΔI_C) at constant emitter current IE.

$$R_o = \frac{\Delta V_{CB}}{\Delta I_C} \quad \text{at constant } I_E$$

Characteristics of CB configuration

- As the output resistance is of very high value, a large change in V_{CB} produces a very little change in collector current I_C.
- This Configuration provides good stability against increase in temperature.
- The CB configuration is used for high frequency applications.

Expression for Collector current

With the above idea, let us try to draw some expression for collector current.

Along with the emitter current flowing, there is some amount of base current I_B which flows through the base terminal due to electron hole recombination. As collector-base junction is reverse biased, there is another current which is flown due to minority charge carriers. This is the leakage current which can be understood as $I_{leakage}$. This is due to minority charge carriers and hence very small.

The emitter current that reaches the collector terminal is

$$\alpha I_E$$

Total collector current

$$I_C = \alpha I_E + I_{leakage}$$

If the emitter-base voltage V_{EB} = 0, even then, there flows a small leakage current, which can be termed as I_{CBO} (collector-base current with output open).

The collector current therefore can be expressed as

$$I_C = \alpha I_E + I_{CBO}$$

$$I_E = I_C + I_B$$

$$I_C = \alpha(I_C + I_B) + I_{CBO}$$

$$I_C(1 - \alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1 - \alpha} I_B + \frac{I_{CBO}}{1 - \alpha}$$

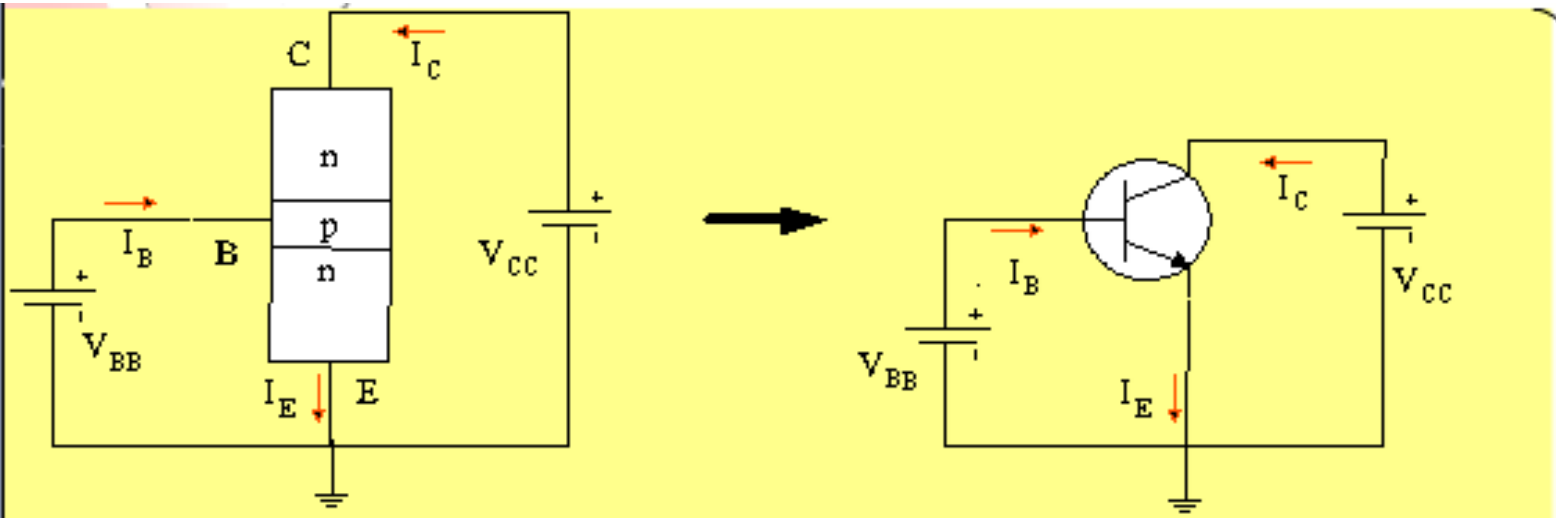
$$I_C = \left(\frac{\alpha}{1 - \alpha}\right) I_B + \left(\frac{1}{1 - \alpha}\right) I_{CBO}$$

The value of collector current depends on base current and leakage current along with the current amplification factor of that transistor in use.

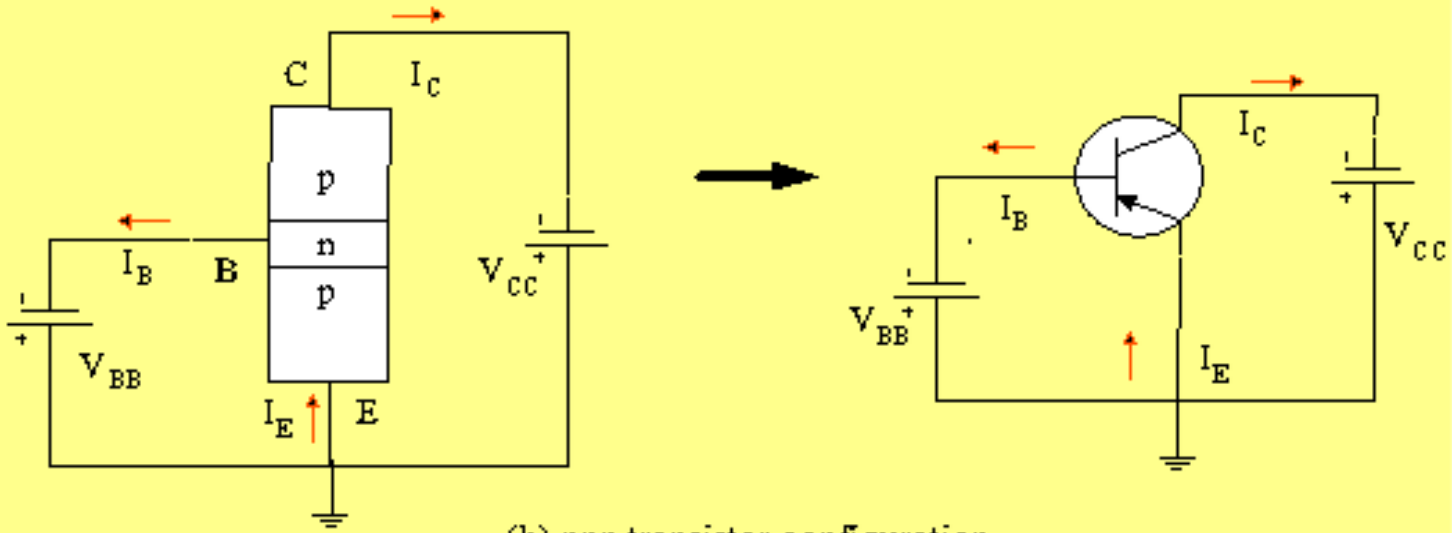
Common-Emitter Configuration

- It is called common-emitter configuration since :
  - emitter is common or reference to both input and output terminals.
  - emitter is usually the terminal closest to or at ground potential.
- Almost amplifier design is using connection of CE due to the high gain for current and voltage.
- Two set of characteristics are necessary to describe the behavior for CE ;input (base terminal) and output (collector terminal) parameters.

Proper Biasing common-emitter configuration in active region



(a) npn transistor configuration



(b) pnp transistor configuration

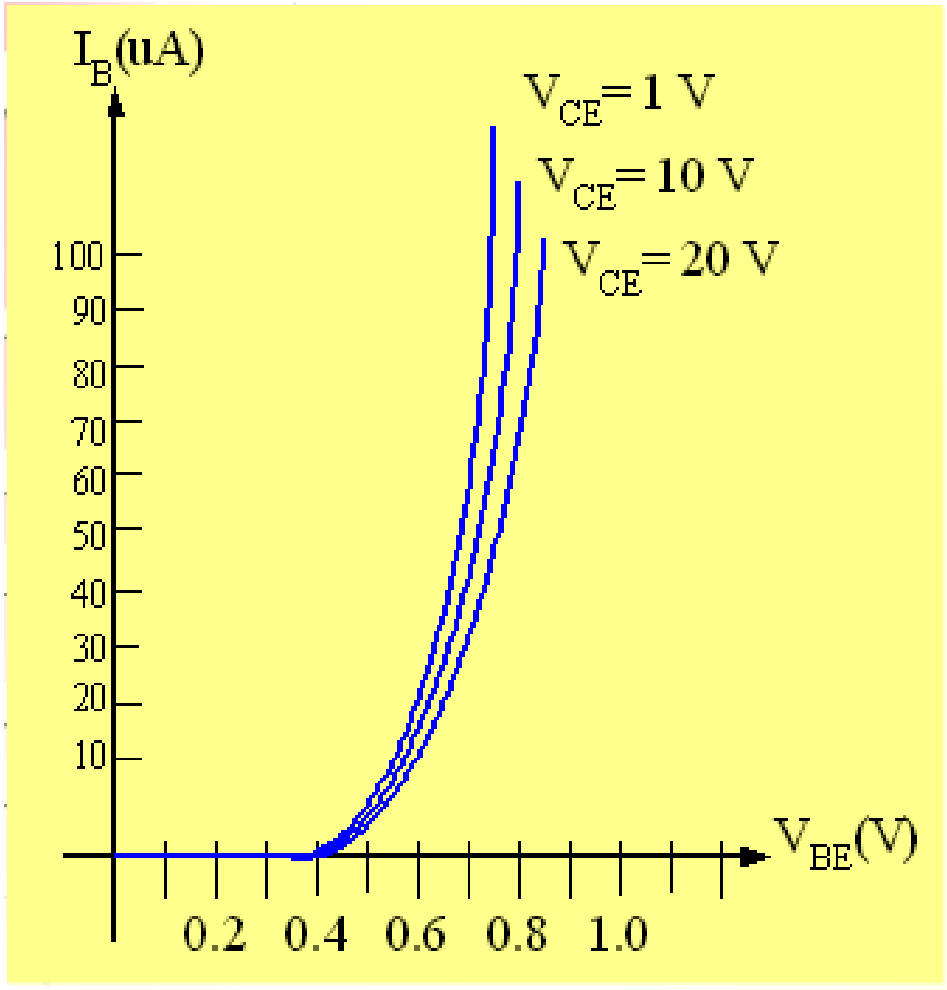
Fig 4.7 : Common-emitter configuration

$$I_E = I_C + I_B$$

Input characteristics

- The input characteristics for the CE configuration of transistor which illustrates the variation in I_B in accordance with V_{BE} when V_{CE} is kept constant.
- From the graph shown in Figure 10 above, the input resistance of the transistor can be obtained as

$$R_{in} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE}=constant}$$



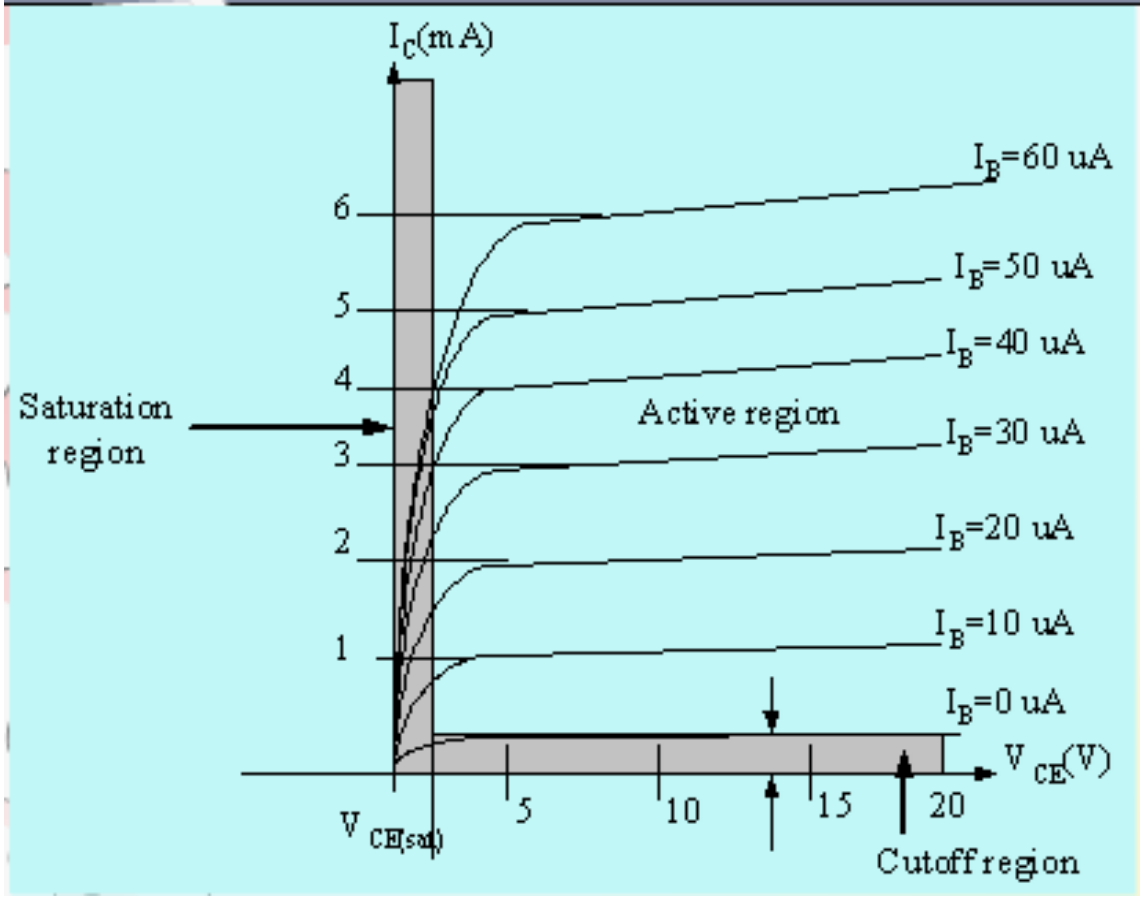
Input characteristics for a common-emitter NPN transistor

- I_B is microamperes compared to miliamperes of I_C.
- I_B will flow when V_{BE} > 0.7V for silicon and 0.3V for germanium
- Before this value I_B is very small and no I_B.
- Base-emitter junction is forward bias
- Increasing V_{CE} will reduce I_B for different values.

Output Characteristics

- The variation in I_C with the changes in V_{CE} when I_B is held constant. From the graph shown, the output resistance can be obtained as:

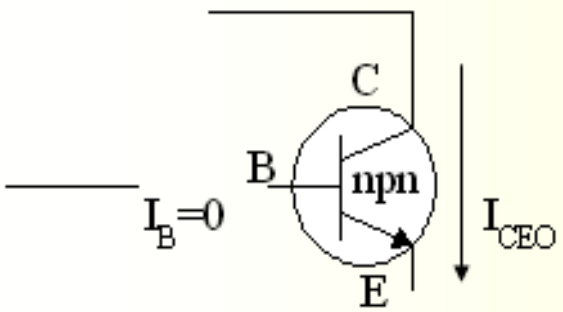
$$R_{out} = \left.\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_B = constant}$$

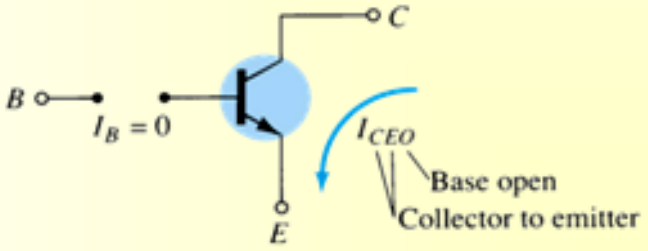


Output characteristics for a common-emitter npn transistor

- For small V_{CE} ($V_{CE} < V_{CESAT}$, I_C increase linearly with increasing of V_{CE}
- $V_{CE} > V_{CESAT}$ I_C not totally depends on V_{CE} → constant I_C
- I_B(uA) is very small compare to I_C (mA). Small increase in I_B cause big increase in I_C
- I_B=0 A → I_{CEO} occur.
- Noticing the value when I_C=0A. There is still some value of current flows.

Active region	Saturation region	Cut-off region
• B-E junction is forward bias • C-B junction is reverse bias • can be employed for voltage, current and power amplification	• B-E and C-B junction is forward bias, thus the values of I_B and I_C is too big. • The value of V_{CE} is so small. • Suitable region when the transistor as a logic switch. • NOT and avoid this region when the transistor as an amplifier.	• region below $I_B=0\mu A$ is to be avoided if an undistorted o/p signal is required • B-E junction and C-B junction is reverse bias • $I_B=0$, I_C not zero, during this condition $I_C=I_{CEO}$ where is this current flow when B-E is reverse bias.





Current Transfer Characteristics

- This characteristic of CE configuration shows the variation of I_C with I_B keeping V_{CE} as a constant. This ratio is referred to as common-emitter current gain and is always greater than 1. This can be mathematically given by

$$\beta = \frac{\Delta I_C}{\Delta I_B}\Big|_{V_{CE}=constant}$$

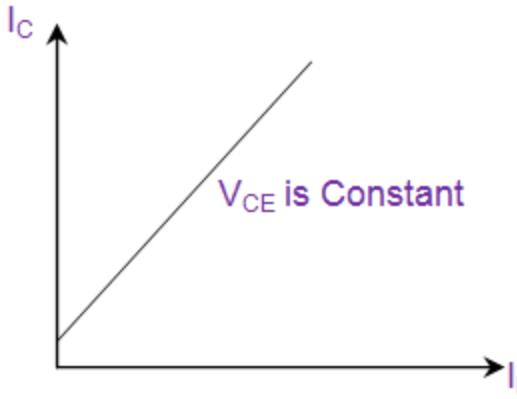


Figure 12 Transfer Characteristics for CE Configuration

Relation between β and α

Let us try to derive the relation between base current amplification factor and emitter current amplification factor.

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

$$I_E = I_B + I_C$$

$$\Delta I_E = \Delta I_B + \Delta I_C$$

$$\Delta I_B = \Delta I_E - \Delta I_C$$

We can write

$$\beta = \frac{\Delta I_C}{\Delta I_E - \Delta I_C}$$

Relation between β and α

Dividing by ΔI_E

$$\beta = \frac{\Delta I_C / \Delta I_E}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}}$$

We have

$$\alpha = \Delta I_C / \Delta I_E$$

Therefore,

$$\beta = \frac{\alpha}{1 - \alpha}$$

From the above equation, it is evident that, as α approaches 1, β reaches infinity.

Hence, **the current gain in Common Emitter connection is very high**. This is the reason this circuit connection is mostly used in all transistor applications.

Expression for Collector Current

In the Common Emitter configuration, I_B is the input current and I_C is the output current.

We know

$$I_E = I_B + I_C$$

And

$$I_C = \alpha I_E + I_{CBO}$$

$$= \alpha(I_B + I_C) + I_{CBO}$$

$$I_C(1 - \alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1 - \alpha} I_B + \frac{1}{1 - \alpha} I_{CBO}$$

If base circuit is open, i.e. if $I_B = 0$,

The collector emitter current with base open is I_{CEO}

$$I_{CEO} = \frac{1}{1 - \alpha} I_{CBO}$$

Expression for Collector Current

Substituting the value of this in the previous equation, we get

$$I_C = \frac{\alpha}{1-\alpha} I_B + I_{CEO}$$

$$I_C = \beta I_B + I_{CEO}$$

Hence the equation for collector current is obtained.

Knee Voltage

- In CE configuration, by keeping the base current I_B constant, if V_{CE} is varied, I_C increases nearly to 1v of V_{CE} and stays constant thereafter. This value of V_{CE} up to which collector current I_C changes with V_{CE} is called the **Knee Voltage**. The transistors while operating in CE configuration, they are operated above this knee voltage.

Characteristics of CE Configuration

- This configuration provides good current gain and voltage gain.
- Keeping V_{CE} constant, with a small increase in V_{BE} the base current I_B increases rapidly than in CB configurations.
- For any value of V_{CE} above knee voltage, I_C is approximately equal to βI_B.
- The input resistance $\mathbf{R_i}$ is the ratio of change in base emitter voltage (ΔV_{BE}) to the change in base current (ΔI_B) at constant collector emitter voltage V_{CE}.

$$R_i = \frac{\Delta V_{BE}}{\Delta I_B} \quad \text{at constant } V_{CE}$$

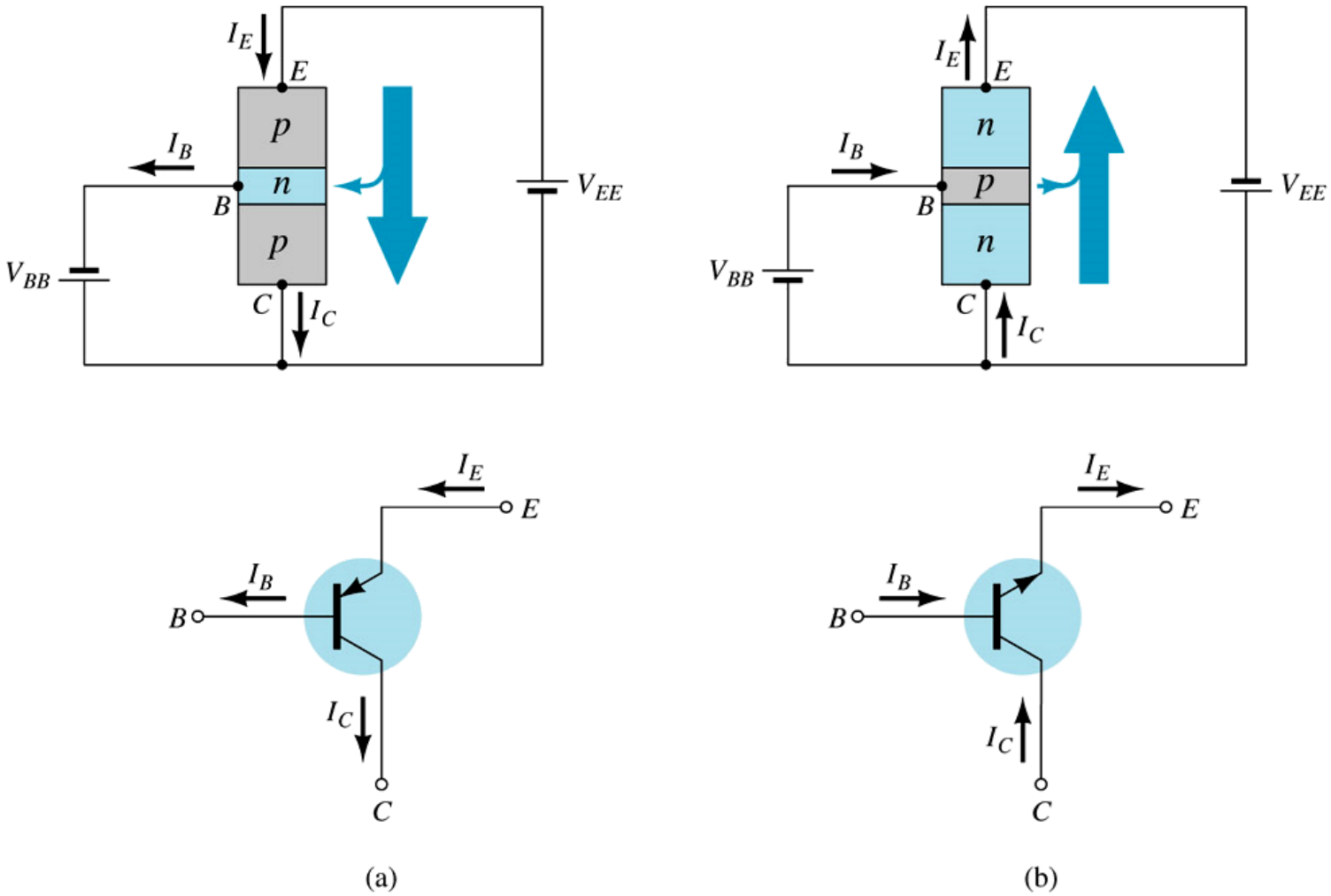
- As the input resistance is of very low value, a small value of V_{BE} is enough to produce a large current flow of base current I_B.
- The output resistance $\mathbf{R_o}$ is the ratio of change in collector emitter voltage (ΔV_{CE}) to the change in collector current (ΔI_C) at constant I_B.

$$R_o = \frac{\Delta V_{CE}}{\Delta I_C} \quad \text{at constant } I_B$$

- As the output resistance of CE circuit is less than that of CB circuit.
- This configuration is usually used for bias stabilization methods and audio frequency applications.

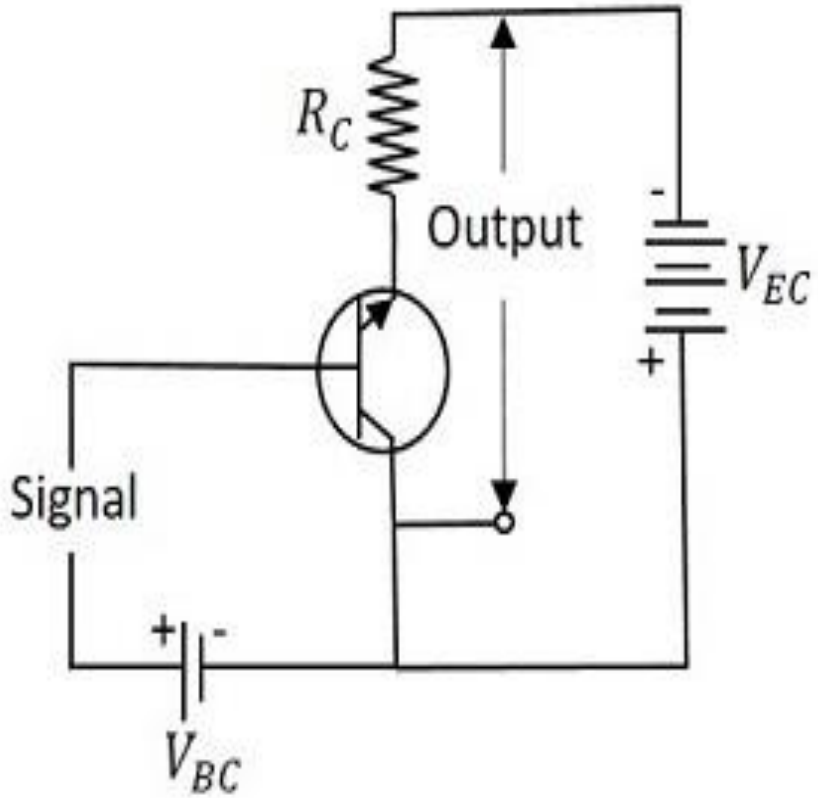
Common – Collector Configuration

- Also called emitter-follower (EF).
- It is called common-emitter configuration since both the signal source and the load share the collector terminal as a common connection point.
- The output voltage is obtained at emitter terminal.
- The input characteristic of common-collector configuration is similar with common-emitter. configuration.
- Common-collector circuit configuration is provided with the load resistor connected from emitter to ground.
- It is used primarily for impedance-matching purpose since it has high input impedance and low output impedance.

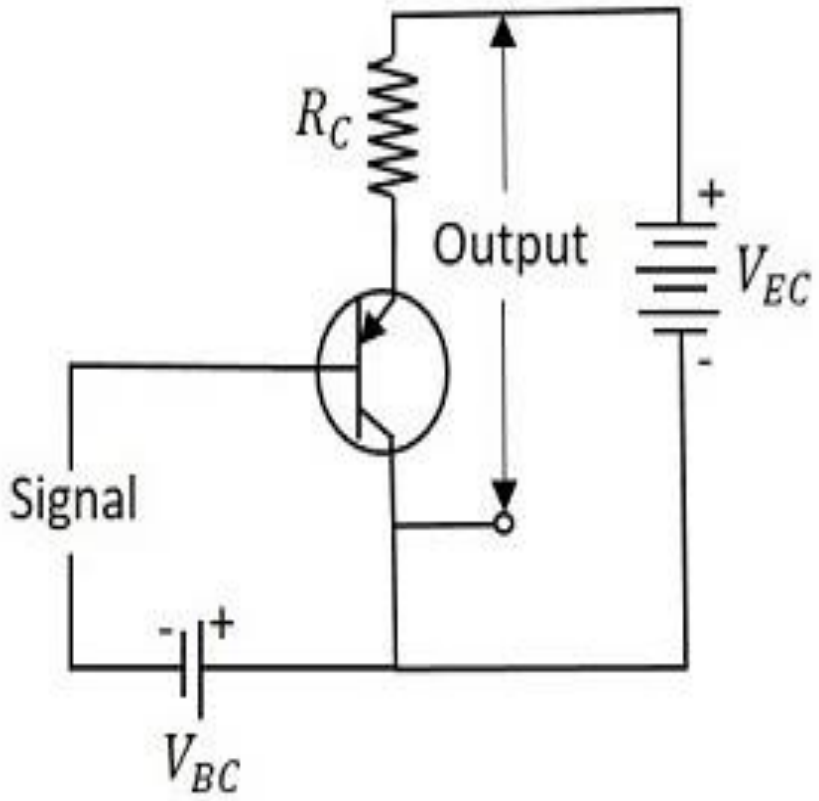


Notation and symbols used with the common-collector configuration: (a) pnp transistor ; (b) npn transistor.

Common Collector (CC) Configuration



Using NPN transistor



Using PNP transistor

Input Characteristics

- the input characteristics for CC configuration which describes the variation in I_B in accordance with V_{CB}, for a constant value of Collector-Emitter voltage, V_{CE}.

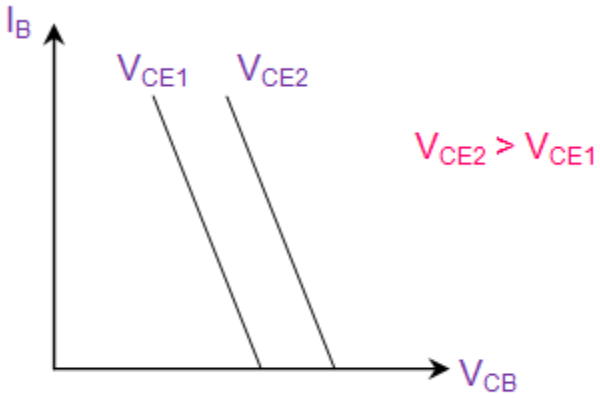


Figure 6 Input Characteristics for CC Configuration

Output Characteristics

- the output characteristics for the CC configuration which exhibit the variations in I_E against the changes in V_{CE} for constant values of I_B.

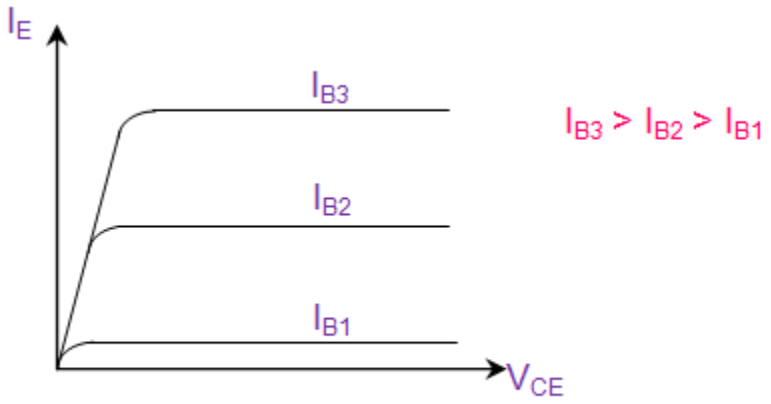
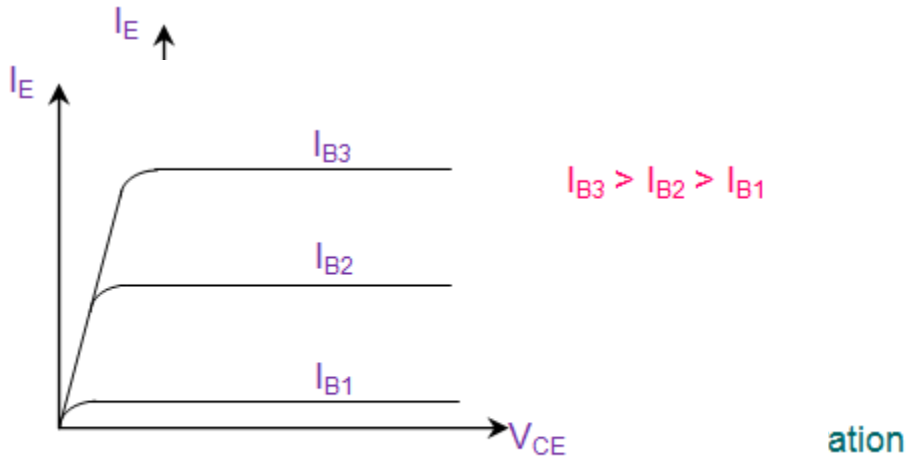


Figure 7 Output Characteristics for CC Configuration

Current Transfer Characteristics

- This characteristic of CC configuration (Figure 8) shows the variation of I_E with I_B keeping V_{CE} as a constant.



Figu ation

Figure 7 Output Characteristics for CC Configuration

Current Amplification Factor (γ)

The ratio of change in emitter current (ΔI_E) to the change in base current (ΔI_B) is known as **Current Amplification factor** in common collector (CC) configuration. It is denoted by γ.

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

- The current gain in CC configuration is same as in CE configuration.
- The voltage gain in CC configuration is always less than 1.

Relation between γ and α

Let us try to draw some relation between γ and α

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

$$I_E = I_B + I_C$$

$$\Delta I_E = \Delta I_B + \Delta I_C$$

$$\Delta I_B = \Delta I_E - \Delta I_C$$

Substituting the value of I_B, we get

$$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$$

Relation between γ and α

Dividing by ΔI_E

$$\gamma = \frac{\Delta I_E / \Delta I_E}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}}$$

$$= \frac{1}{1 - \alpha}$$

$$\gamma = \frac{1}{1 - \alpha}$$

Expression for collector current

We know

$$I_C = \alpha I_E + I_{CBO}$$

$$I_E = I_B + I_C = I_B + (\alpha I_E + I_{CBO})$$

$$I_E(1-\alpha) = I_B + I_{CBO}$$

$$I_E = \frac{I_B}{1-\alpha} + \frac{I_{CBO}}{1-\alpha}$$

$$I_C \cong I_E = (\beta+1)I_B + (\beta+1)I_{CBO}$$

The above is the expression for collector current.

Characteristics of CC Configuration

- This configuration provides current gain but no voltage gain.
- In CC configuration, the input resistance is high and the output resistance is low.
- The voltage gain provided by this circuit is less than 1.
- The sum of collector current and base current equals emitter current.
- The input and output signals are in phase.
- This configuration works as non-inverting amplifier output.
- This circuit is mostly used for impedance matching. That means, to drive a low impedance load from a high impedance source.

Transistor Regions of Operation

- The DC supply is provided for the operation of a transistor. This DC supply is given to the two PN junctions of a transistor which influences the actions of majority carriers in these emitter and collector junctions.
- The junctions are forward biased and reverse biased based on our requirement. **Forward biased** is the condition where a positive voltage is applied to the p-type and negative voltage is applied to the n-type material. **Reverse biased** is the condition where a positive voltage is applied to the n-type and negative voltage is applied to the p-type material.

Transistor Regions of Operation

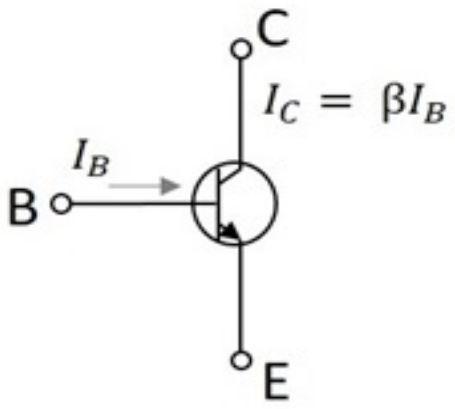
These biasing methods make the transistor circuit to work in four kinds of regions such as **Active region**, **Saturation region**, **Cutoff region** and **Inverse active region** (seldom used). This is understood by having a look at the following table.

Emitter Junction	Collector Junction	Region of Operation
Forward biased	Forward biased	Saturation region
Forward biased	Reverse biased	Active region
Reverse biased	Forward biased	Inverse active region
Reverse biased	Reverse biased	Cut off region

Active Region

This is the region in which transistors have many applications. This is also called as **linear region**. A transistor while in this region, acts better as an **Amplifier**.

The following circuit diagram shows a transistor working in active region.



This region lies between saturation and cutoff. The transistor operates in active region when the emitter junction is forward biased and collector junction is reverse biased.

In the active state, collector current is β times the base current, i.e.

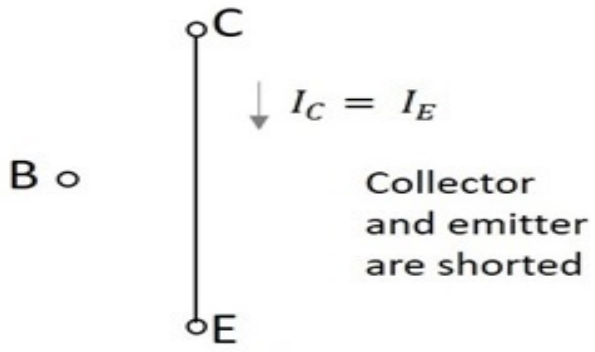
$$I_C = \beta I_B$$

Where I_C = collector current, β = current amplification factor, and I_B = base current.

Saturation Region

This is the region in which transistor tends to behave as a closed switch. The transistor has the effect of its collector and emitter being shorted. The collector and emitter currents are maximum in this mode of operation.

The following figure shows a transistor working in saturation region.



The transistor operates in saturation region when both the emitter and collector junctions are forward biased.

In saturation mode,

$$\beta < \frac{I_C}{I_B}$$

As in the saturation region the transistor tends to behave as a closed switch,

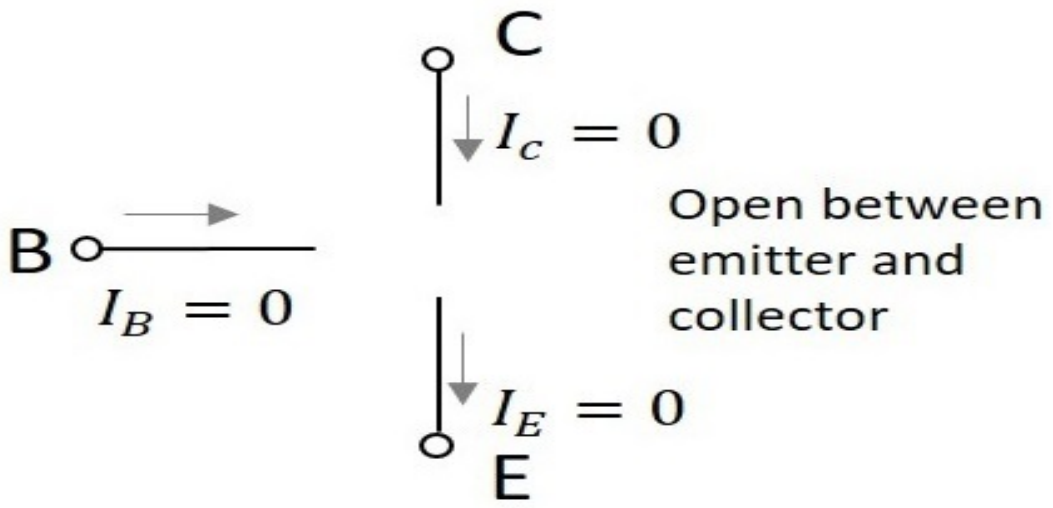
$$I_C = I_E$$

Where I_C = collector current and I_E = emitter current.

Cut off Region

This is the region in which transistor tends to behave as an open switch. The transistor has the effect of its collector and base being opened. The collector, emitter and base currents are all zero in this mode of operation.

The figure below shows a transistor working in cutoff region.



The transistor operates in cutoff region when both the emitter and collector junctions are reverse biased.

As in cutoff region, the collector current, emitter current and base currents are nil, we can write as

$$I_C = I_E = I_B = 0$$

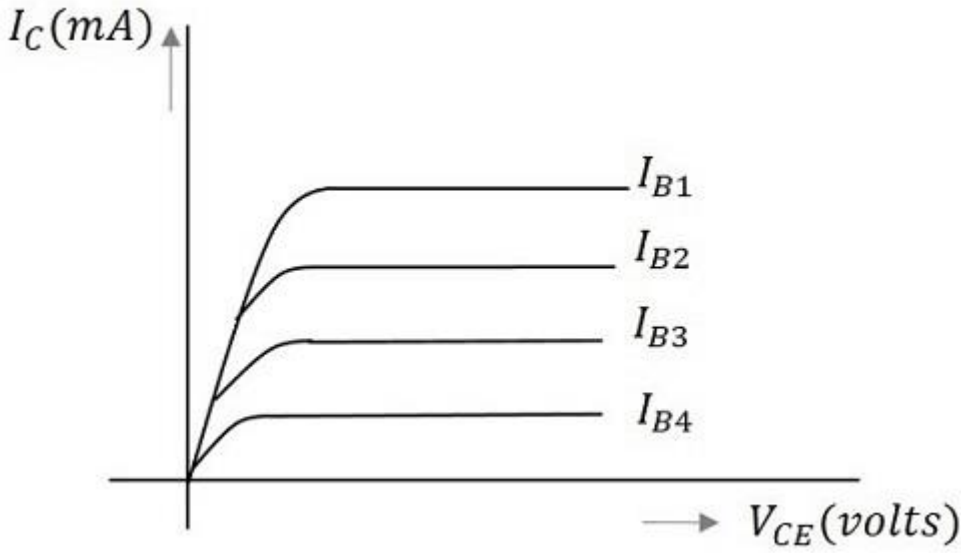
Where I_C = collector current, I_E = emitter current, and I_B = base current.

Transistor Load Line Analysis

- Among all these regions, we have found that the transistor operates well in active region and hence it is also called as **linear region**. The outputs of the transistor are the collector current and collector voltages.

Transistor Load Line Analysis

- The output characteristics are drawn between collector current $\mathbf{I_C}$ and collector voltage $\mathbf{V_{CE}}$ for different values of base current $\mathbf{I_B}$.

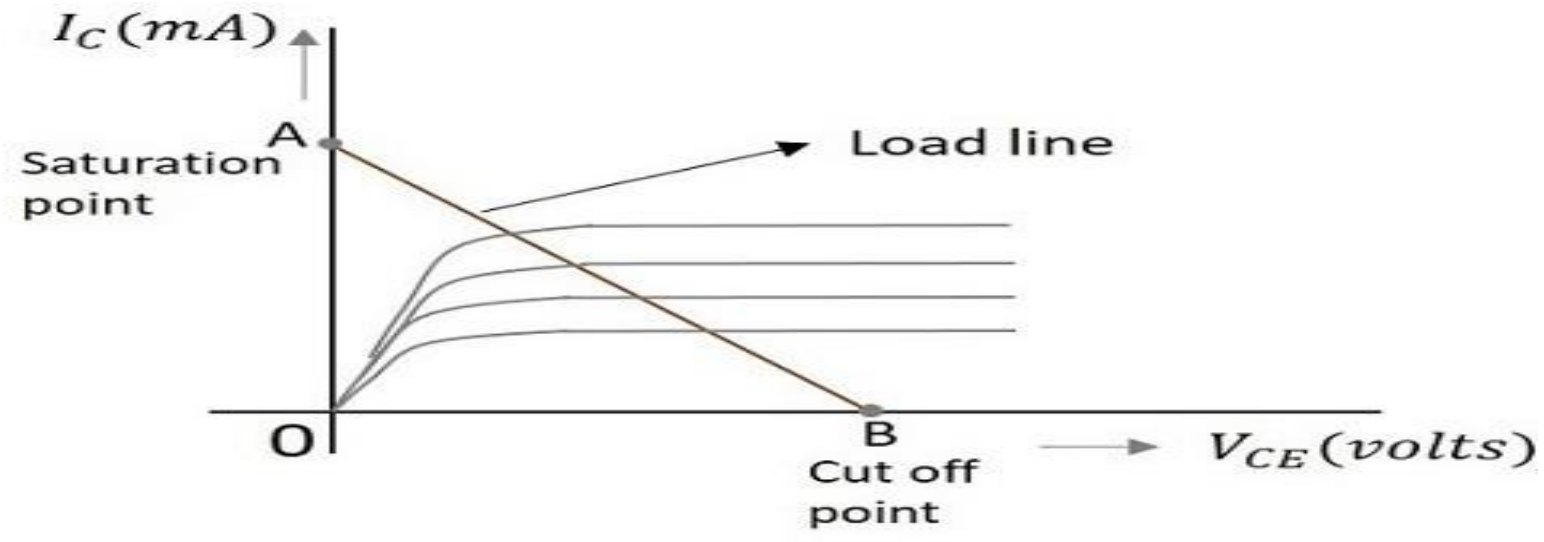


Load Line

- When a value for the maximum possible collector current is considered, that point will be present on the Y-axis, which is nothing but the **Saturation point**. As well, when a value for the maximum possible collector emitter voltage is considered, that point will be present on the X-axis, which is the **Cutoff point**.
- When a line is drawn joining these two points, such a line can be called as **Load line**. This is called so as it symbolizes the output at the load. This line, when drawn over the output characteristic curve, makes contact at a point called as **Operating point** or **quiescent point** or simply **Q-point**.

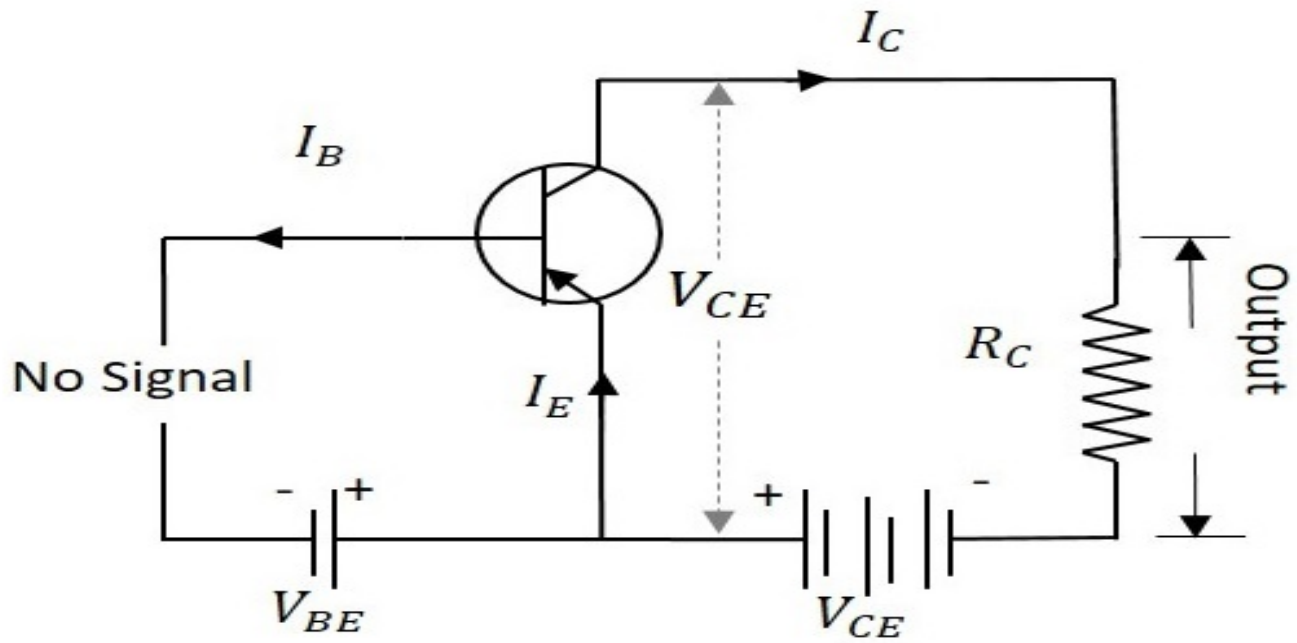
Load Line

The load line is drawn by joining the saturation and cut off points. The region that lies between these two is the **linear region**. A transistor acts as a good amplifier in this linear region. If this load line is drawn only when DC biasing is given to the transistor, but **no input** signal is applied, then such a load line is called as **DC load line**. Whereas the load line drawn under the conditions when an **input signal** along with the DC voltages are applied, such a line is called as an **AC load line**.



DC Load Line

When the transistor is given the bias and no signal is applied at its input, the load line drawn under such conditions, can be understood as **DC** condition. Here there will be no amplification as the **signal is absent**. The circuit will be as shown below.

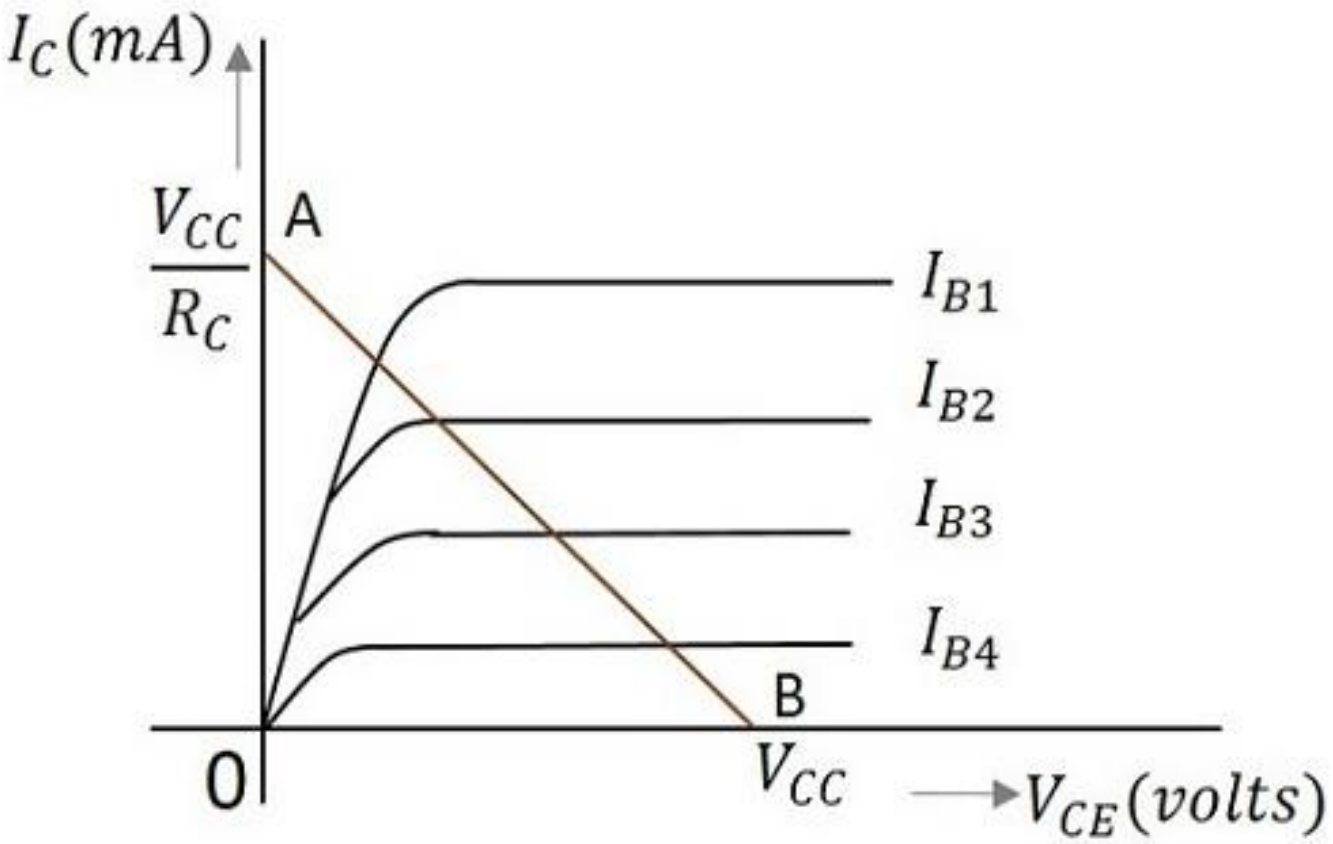


The value of collector emitter voltage at any given time will be

$$V_{CE} = V_{CC} - I_C R_C$$

As V_{CC} and R_C are fixed values, the above one is a first degree equation and hence will be a straight line on the output characteristics. This line is called as **D.C. Load line**.

DC Load Line



To obtain the load line, the two end points of the straight line are to be determined. Let those two points be A and B.

DC Load Line

To obtain A

When collector emitter voltage V_{CE} = 0, the collector current is maximum and is equal to V_{CC}/R_C. This gives the maximum value of V_{CE}. This is shown as

$$V_{CE} = V_{CC} - I_C R_C$$

$$0 = V_{CC} - I_C R_C$$

$$I_C = V_{CC}/R_C$$

This gives the point A (OA = V_{CC}/R_C) on collector current axis, shown in the above figure.

DC Load Line

To obtain B

When the collector current $I_C = 0$, then collector emitter voltage is maximum and will be equal to the V_{CC}. This gives the maximum value of I_C. This is shown as

$$V_{CE} = V_{CC} - I_C R_C$$

$$= V_{CC}$$

(AS $I_C = 0$)

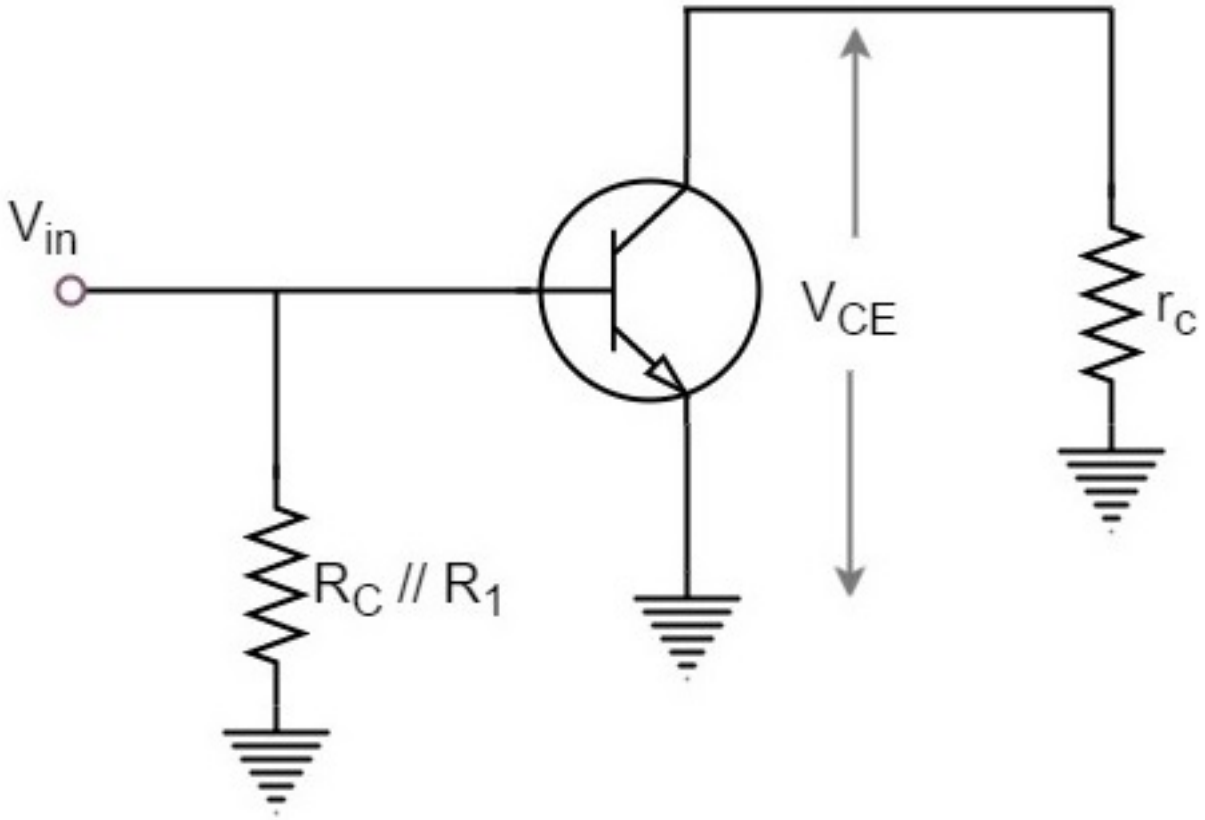
This gives the point B, which means (OB = V_{CC}) on the collector emitter voltage axis shown in the above figure.

Hence we got both the saturation and cutoff point determined and learnt that the load line is a straight line. So, a DC load line can be drawn.

AC Load Line

The DC load line discussed previously, analyzes the variation of collector currents and voltages, when no AC voltage is applied. Whereas the AC load line gives the peak-to-peak voltage, or the maximum possible output swing for a given amplifier.

We shall consider an AC equivalent circuit of a CE amplifier for our understanding.



AC Load Line

From the above figure,

$$V_{CE} = (R_C // R_1) \times I_C$$

$$r_C = R_C // R_1$$

For a transistor to operate as an amplifier, it should stay in active region. The quiescent point is so chosen in such a way that the maximum input signal excursion is symmetrical on both negative and positive half cycles.

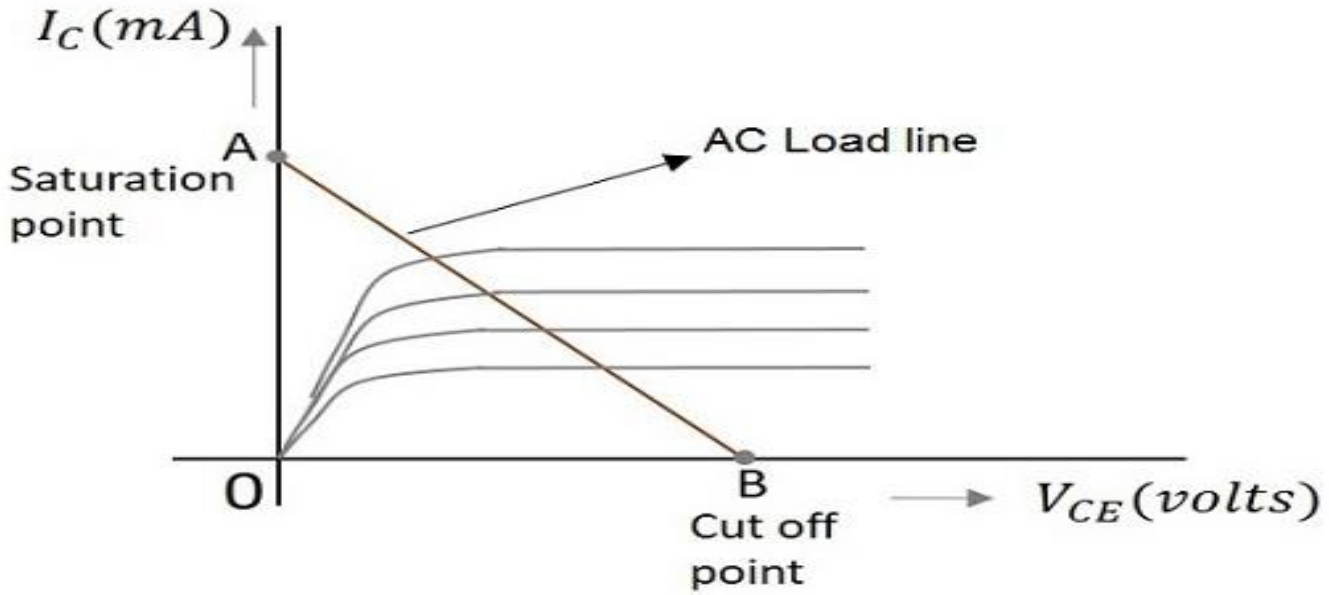
Hence,

$$V_{max} = V_{CEQ} \quad \text{and} \quad V_{min} = -V_{CEQ}$$

Where V_{CEQ} is the emitter-collector voltage at quiescent point

AC Load Line

The following graph represents the AC load line which is drawn between saturation and cut off points.



From the graph above, the current IC at the saturation point is

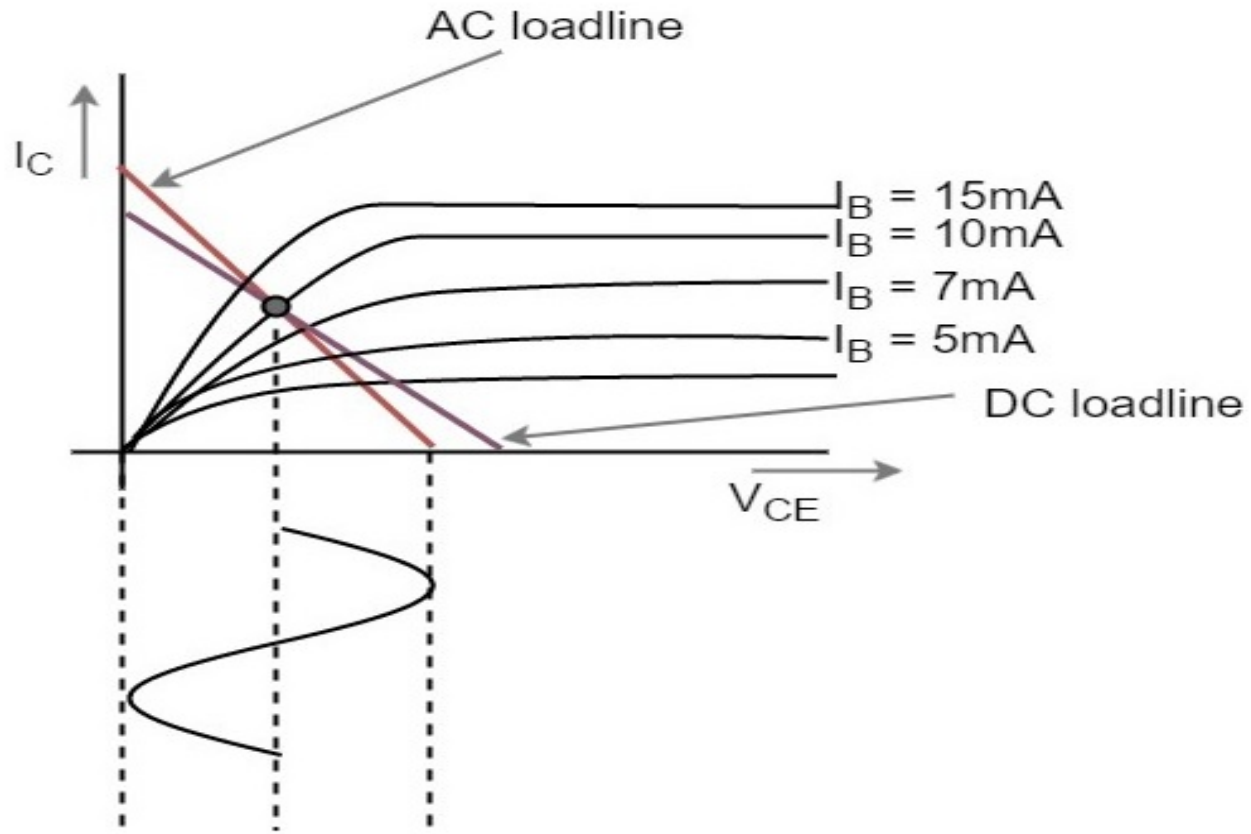
$$I_{C(sat)} = I_{CQ} + (V_{CEQ}/r_C)$$

The voltage V_{CE} at the cutoff point is

$$V_{CE(off)} = V_{CEQ} + I_{CQ}r_C$$

AC and DC Load Line

When AC and DC Load lines are represented in a graph, it can be understood that they are not identical. Both of these lines intersect at the **Q-point** or **quiescent point**. The endpoints of AC load line are saturation and cut off points. This is understood from the figure below.



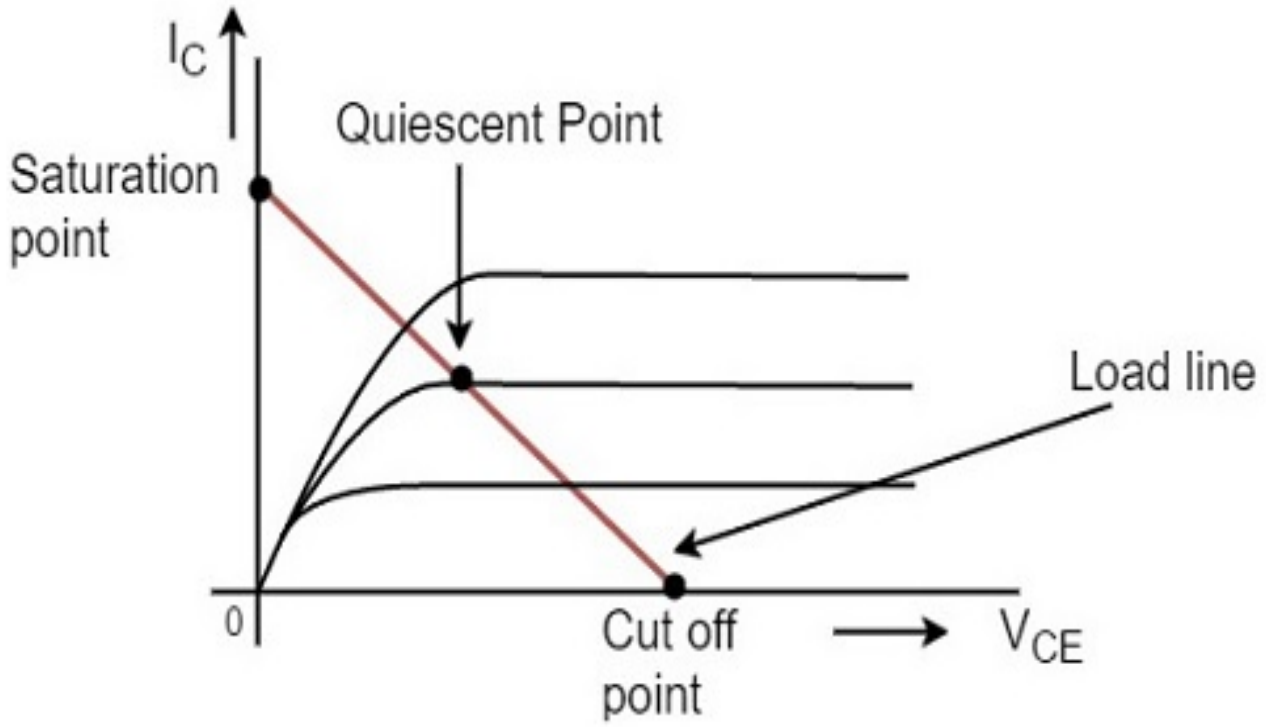
From the above figure, it is understood that the quiescent point (the dark dot) is obtained when the value of base current IB is 10mA. This is the point where both the AC and DC load lines intersect.

Operating Point

- When a line is drawn joining the saturation and cut off points, such a line can be called as **Load line**. This line, when drawn over the output characteristic curve, makes contact at a point called as **Operating point**.
- This operating point is also called as **quiescent point** or simply **Q-point**. There can be many such intersecting points, but the Q-point is selected in such a way that irrespective of AC signal swing, the transistor remains in the active region.

Operating Point

The following graph shows how to represent the operating point.

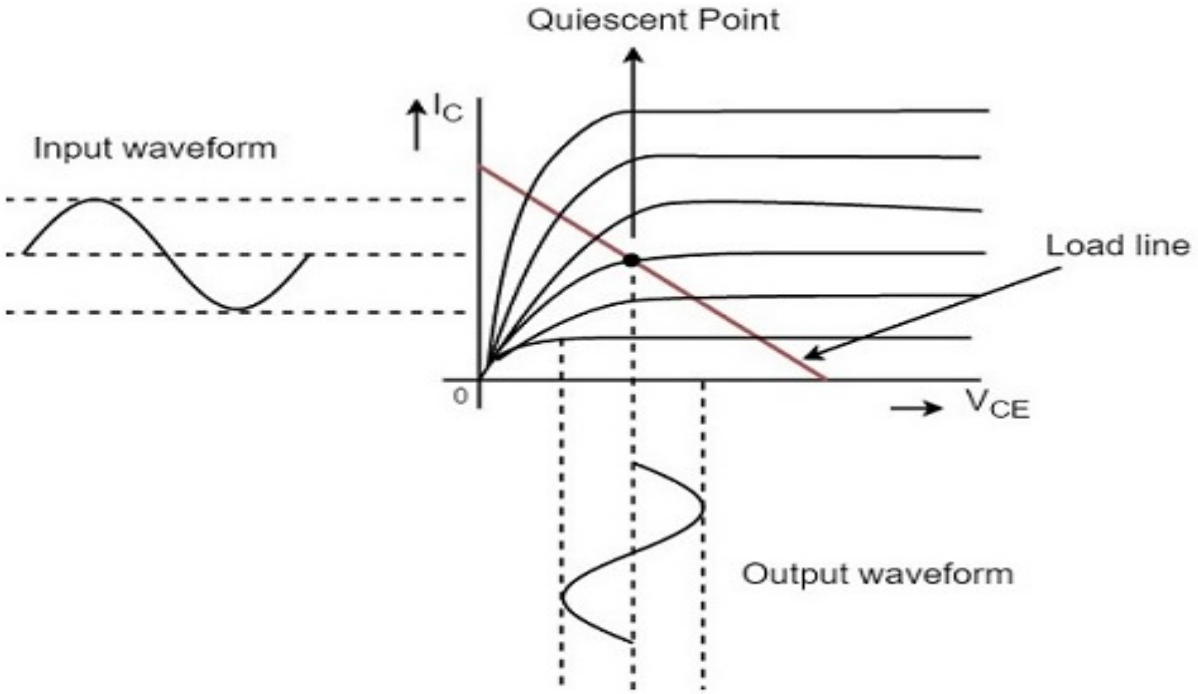


The operating point should not get disturbed as it should remain stable to achieve faithful amplification. Hence the quiescent point or Q-point is the value where the **Faithful Amplification** is achieved.

Faithful Amplification

The process of increasing the signal strength is called as **Amplification**. This amplification when done without any loss in the components of the signal, is called as **Faithful amplification**.

Faithful amplification is the process of obtaining complete portions of input signal by increasing the signal strength. This is done when AC signal is applied at its input.

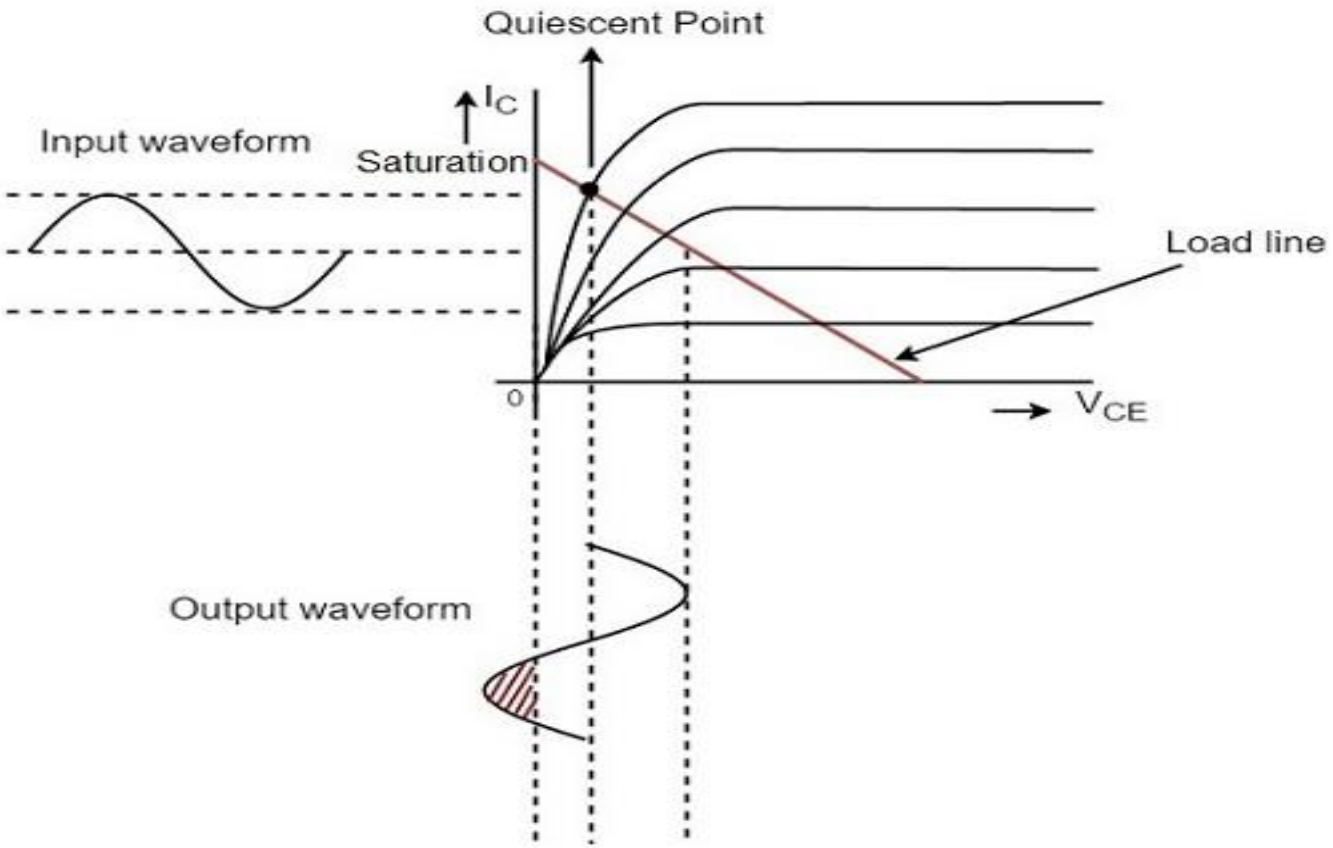


In the above graph, the input signal applied is completely amplified and reproduced without any losses. This can be understood as **Faithful Amplification**.

The operating point is so chosen such that it lies in the **active region** and it helps in the reproduction of complete signal without any loss.

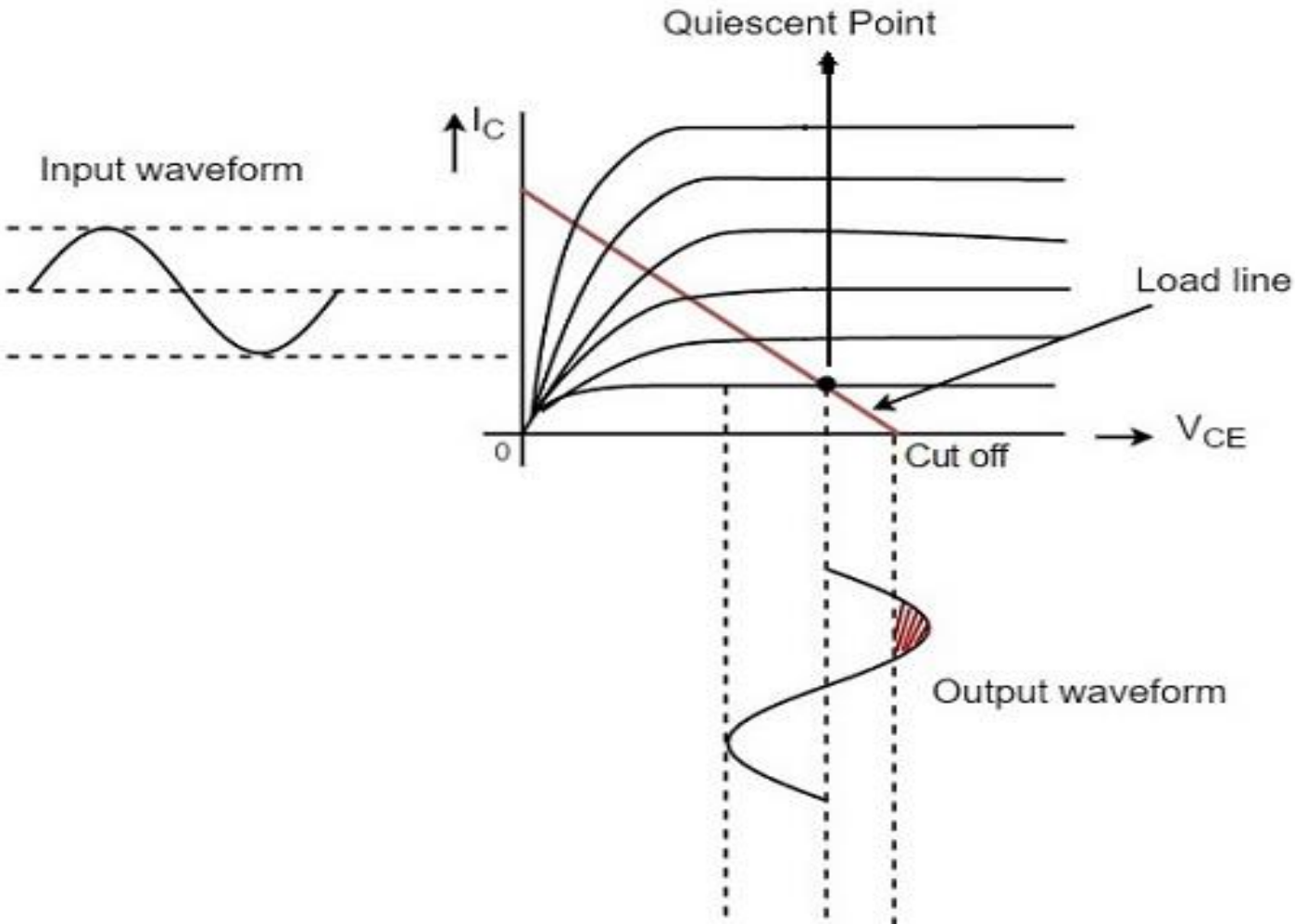
Faithful Amplification

If the operating point is considered near saturation point, then the amplification will be as under.



Faithful Amplification

If the operation point is considered near cut off point, then the amplification will be as under.



Methods of Transistor Biasing

- The biasing in transistor circuits is done by using two DC sources V_{BB} and V_{CC}. It is economical to minimize the DC source to one supply instead of two which also makes the circuit simple.
- The commonly used methods of transistor biasing are
- Base Resistor method
- Collector to Base bias
- Biasing with Collector feedback resistor
- Voltage-divider bias
- All of these methods have the same basic principle of obtaining the required value of I_B and I_C from V_{CC} in the zero signal conditions.

Base Resistor Method

- In this method, a resistor R_B of high resistance is connected in base, as the name implies. The required zero signal base current is provided by V_{CC} which flows through R_B. The base emitter junction is forward biased, as base is positive with respect to emitter.
- The required value of zero signal base current and hence the collector current (as $I_C = \beta I_B$) can be made to flow by selecting the proper value of base resistor RB. Hence the value of R_B is to be known.

Base Resistor Method

Let I_C be the required zero signal collector current. Therefore,

$$I_B = \frac{I_C}{\beta}$$

Considering the closed circuit from V_{CC}, base, emitter and ground, while applying the Kirchhoff's voltage law, we get,

$$V_{CC} = I_B R_B + V_{BE}$$

Or

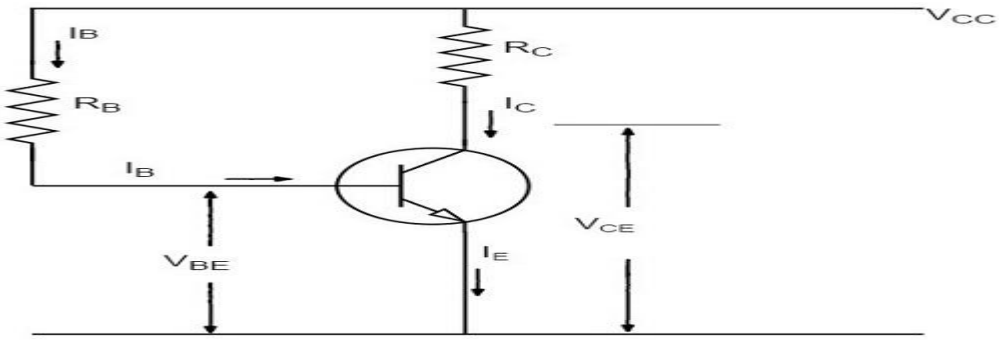
$$I_B R_B = V_{CC} - V_{BE}$$

Therefore

$$R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

Since V_{BE} is generally quite small as compared to V_{CC}, the former can be neglected with little error. Then,

$$R_B = \frac{V_{CC}}{I_B}$$



Collector to Base Bias

- The collector to base bias circuit is same as base bias circuit except that the base resistor R_B is returned to collector, rather than to V_{CC} supply
- This circuit helps in improving the stability considerably. If the value of I_C increases, the voltage across R_L increases and hence the V_{CE} also increases. This in turn reduces the base current I_B. This action somewhat compensates the original increase.

Collector to Base Bias

Voltage drop across R_L will be

$$R_L = (I_C + I_B)R_L \cong I_C R_L$$

From the figure,

$$I_C R_L + I_B R_B + V_{BE} = V_{CC}$$

Or

$$I_B R_B = V_{CC} - V_{BE} - I_C R_L$$

Therefore

$$R_B = \frac{V_{CC} - V_{BE} - I_C R_L}{I_B}$$

Or

$$R_B = \frac{(V_{CC} - V_{BE} - I_C R_L)\beta}{I_C}$$

Collector to Base Bias

Applying KVL we have

$$(I_B + I_C)R_L + I_B R_B + V_{BE} = V_{CC}$$

Or

$$I_B(R_L + R_B) + I_C R_L + V_{BE} = V_{CC}$$

Therefore

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_L}{R_L + R_B}$$

Biasing with Collector Feedback resistor

- In this method, the base resistor R_B has its one end connected to base and the other to the collector as its name implies. In this circuit, the zero signal base current is determined by V_{CB} but not by V_{CC}.
- It is clear that V_{CB} forward biases the base-emitter junction and hence base current I_B flows through R_B. This causes the zero signal collector current to flow in the circuit.

Biasing with Collector Feedback resistor

The required value of R_B needed to give the zero signal current I_C can be determined as follows.

$$V_{CC} = I_C R_C + I_B R_B + V_{BE}$$

Or

$$R_B = \frac{V_{CC} - V_{BE} - I_C R_C}{I_B}$$

$$= \frac{V_{CC} - V_{BE} - \beta I_B R_C}{I_B}$$

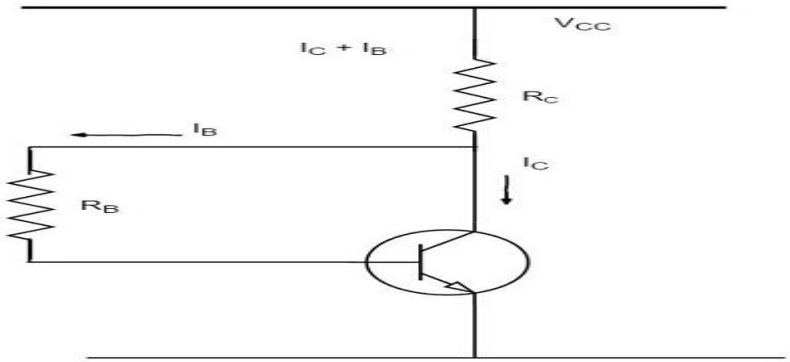
Since $I_C = \beta I_B$

Alternatively,

$$V_{CE} = V_{BE} + V_{CB}$$

Or

$$V_{CB} = V_{CE} - V_{BE}$$



Biasing with Collector Feedback resistor

Since

$$R_B = \frac{V_{CB}}{I_B} = \frac{V_{CE} - V_{BE}}{I_B}$$

Where

$$I_B = \frac{I_C}{\beta}$$

Voltage Divider Bias Method

- Among all the methods of providing biasing and stabilization, the **voltage divider bias method** is the most prominent one. Here, two resistors R_1 and R_2 are employed, which are connected to V_{CC} and provide biasing. The resistor R_E employed in the emitter provides stabilization.
- The name voltage divider comes from the voltage divider formed by R_1 and R_2. The voltage drop across R_2 forward biases the base-emitter junction. This causes the base current and hence collector current flow in the zero signal conditions.

Voltage Divider Bias Method

Collector Current, I_C

From the circuit, it is evident that,

$$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

Therefore, the voltage across resistance R_2 is

$$V_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2$$

Applying Kirchhoff's voltage law to the base circuit,

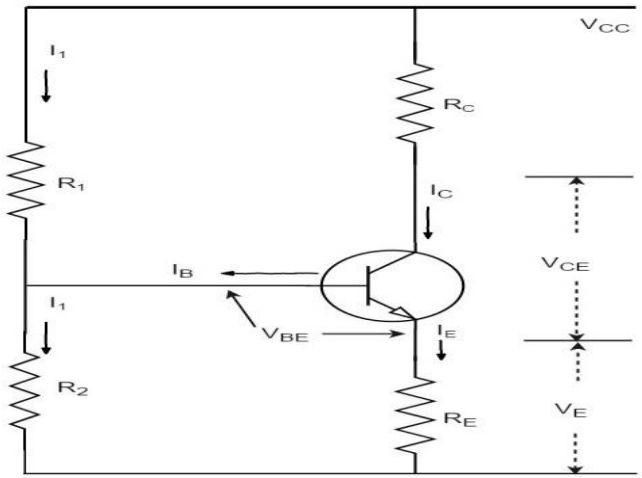
$$V_2 = V_{BE} + V_E$$

$$V_2 = V_{BE} + I_E R_E$$

$$I_E = \frac{V_2 - V_{BE}}{R_E}$$

Since $I_E \approx I_C$,

$$I_C = \frac{V_2 - V_{BE}}{R_E}$$



Voltage Divider Bias Method

Collector-Emitter Voltage, V_{CE}

Applying Kirchhoff's voltage law to the collector side,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

Since $I_E \cong I_C$

$$= I_C R_C + V_{CE} + I_C R_E$$

$$= I_C (R_C + R_E) + V_{CE}$$

Therefore,

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

R_E provides excellent stabilization in this circuit.

$$V_2 = V_{BE} + I_C R_E$$

Voltage Divider Bias Method

- It is evident that I_C doesn't depend upon β. V_{BE} is very small that I_C doesn't get affected by V_{BE} at all. Thus I_C in this circuit is almost independent of transistor parameters and hence good stabilization is achieved.
- Suppose there is a rise in temperature, then the collector current I_C decreases, which causes the voltage drop across R_E to increase. As the voltage drop across R_2 is V_2, which is independent of I_C, the value of V_{BE} decreases. The reduced value of I_B tends to restore I_C to the original value.

Amplifiers Classification

- Based on number of stages
- Depending upon the number of stages of Amplification, there are Single-stage amplifiers and Multi-stage amplifiers.
- **Single-stage Amplifiers** – This has only one transistor circuit, which is a singlestage amplification.
- **Multi-stage Amplifiers** – This has multiple transistor circuit, which provides multi-stage amplification.

Based on its output

- Depending upon the parameter that is amplified at the output, there are voltage and power amplifiers.
- **Voltage Amplifiers** – The amplifier circuit that increases the voltage level of the input signal, is called as Voltage amplifier.
- **Power Amplifiers** – The amplifier circuit that increases the power level of the input signal, is called as Power amplifier.

Based on the input signals

- Depending upon the magnitude of the input signal applied, they can be categorized as Small signal and large signal amplifiers.
- **Small signal Amplifiers** – When the input signal is so weak so as to produce small fluctuations in the collector current compared to its quiescent value, the amplifier is known as Small signal amplifier.
- **Large signal amplifiers** – When the fluctuations in collector current are large i.e. beyond the linear portion of the characteristics, the amplifier is known as large signal amplifier.

Based on the frequency range

- Depending upon the frequency range of the signals being used, there are audio and radio amplifiers.
- **Audio Amplifiers** – The amplifier circuit that amplifies the signals that lie in the audio frequency range i.e. from 20Hz to 20 KHz frequency range, is called as audio amplifier.
- **Power Amplifiers** – The amplifier circuit that amplifies the signals that lie in a very high frequency range, is called as Power amplifier.

Based on Biasing Conditions

- Depending upon their mode of operation, there are class A, class B and class C amplifiers.
- **Class A amplifier** − The biasing conditions in class A power amplifier are such that the collector current flows for the entire AC signal applied.
- **Class B amplifier** − The biasing conditions in class B power amplifier are such that the collector current flows for half-cycle of input AC signal applied.
- **Class C amplifier** − The biasing conditions in class C power amplifier are such that the collector current flows for less than half cycle of input AC signal applied.
- **Class AB amplifier** − The class AB power amplifier is one which is created by combining both class A and class B in order to have all the advantages of both the classes and to minimize the problems they have.

Based on the Coupling method

- Depending upon the method of coupling one stage to the other, there are RC coupled, Transformer coupled and direct coupled amplifier.
- **RC Coupled amplifier** − A Multi-stage amplifier circuit that is coupled to the next stage using resistor and capacitor (RC) combination can be called as a RC coupled amplifier.
- **Transformer Coupled amplifier** − A Multi-stage amplifier circuit that is coupled to the next stage, with the help of a transformer, can be called as a Transformer coupled amplifier.
- **Direct Coupled amplifier** − A Multi-stage amplifier circuit that is coupled to the next stage directly, can be called as a direct coupled amplifier.

Based on the Transistor Configuration

- Depending upon the type of transistor configuration, there are CE CB and CC amplifiers.
- **CE amplifier** – The amplifier circuit that is formed using a CE configured transistor combination is called as CE amplifier.
- **CB amplifier** – The amplifier circuit that is formed using a CB configured transistor combination is called as CB amplifier.
- **CC amplifier** – The amplifier circuit that is formed using a CC configured transistor combination is called as CC amplifier.

Transistor as an Amplifier

- A transistor acts as an amplifier by raising the strength of a weak signal. The DC bias voltage applied to the emitter base junction, makes it remain in forward biased condition. This forward bias is maintained regardless of the polarity of the signal.

Input Resistance

As the input circuit is forward biased, the input resistance will be low. The input resistance is the opposition offered by the base-emitter junction to the signal flow.

By definition, it is the ratio of small change in base-emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage.

$$\text{Input resistance, } R_i = \frac{\Delta V_{BE}}{\Delta I_B}$$

Where R_i = input resistance, V_{BE} = base-emitter voltage, and I_B = base current.

Output Resistance

The output resistance of a transistor amplifier is very high. The collector current changes very slightly with the change in collector-emitter voltage.

By definition, it is the ratio of change in collector-emitter voltage (ΔV_{CE}) to the resulting change in collector current (ΔI_C) at constant base current.

$$\text{Output resistance} = R_o = \frac{\Delta V_{CE}}{\Delta I_C}$$

Where R_0 = Output resistance, V_{CE} = Collector-emitter voltage, and I_C = Collector-emitter voltage.

Effective Collector Load

The load is connected at the collector of a transistor and for a single-stage amplifier, the output voltage is taken from the collector of the transistor and for a multi-stage amplifier, the same is collected from a cascaded stages of transistor circuit.

By definition, it is the total load as seen by the a.c. collector current. In case of single stage amplifiers, the effective collector load is a parallel combination of R_C and R_o.

$$\text{Effective Collector Load, } \quad R_{AC} = R_C // R_o$$

$$= \frac{R_C \times R_o}{R_C + R_o} = R_{AC}$$

Hence for a single stage amplifier, effective load is equal to collector load R_C.

In a multi-stage amplifier (i.e. having more than one amplification stage), the input resistance R_i of the next stage also comes into picture.

Effective collector load becomes parallel combination of R_C, R_o and R_i i.e,

$$\text{Effective Collector Load, } \quad R_{AC} = R_C // R_o // R_i$$

$$R_C // R_i = \frac{R_C R_i}{R_C + R_i}$$

As input resistance R_i is quite small, therefore effective load is reduced.

Current Gain

The gain in terms of current when the changes in input and output currents are observed, is called as **Current gain**. By definition, it is the ratio of change in collector current (ΔI_C) to the change in base current (ΔI_B).

$$\text{Current gain, } \beta = \frac{\Delta I_C}{\Delta I_B}$$

The value of β ranges from 20 to 500. The current gain indicates that input current becomes β times in the collector current.

Voltage Gain

The gain in terms of voltage when the changes in input and output currents are observed, is called as **Voltage gain**. By definition, it is the ratio of change in output voltage (ΔV_{CE}) to the change in input voltage (ΔV_{BE}).

$$\text{Voltage gain, } A_V = \frac{\Delta V_{CE}}{\Delta V_{BE}}$$

$$= \frac{Change\ in\ output\ current \times effective\ load}{Change\ in\ input\ current \times input\ resistance}$$

$$= \frac{\Delta I_C \times R_{AC}}{\Delta I_B \times R_i} = \frac{\Delta I_C}{\Delta I_B} \times \frac{R_{AC}}{R_i} = \beta \times \frac{R_{AC}}{R_i}$$

For a single stage, $R_{AC} = R_C$.

However, for Multistage,

$$R_{AC} = \frac{R_C \times R_i}{R_C + R_i}$$

Where R_i is the input resistance of the next stage.

Power Gain

The gain in terms of power when the changes in input and output currents are observed, is called as **Power gain**.

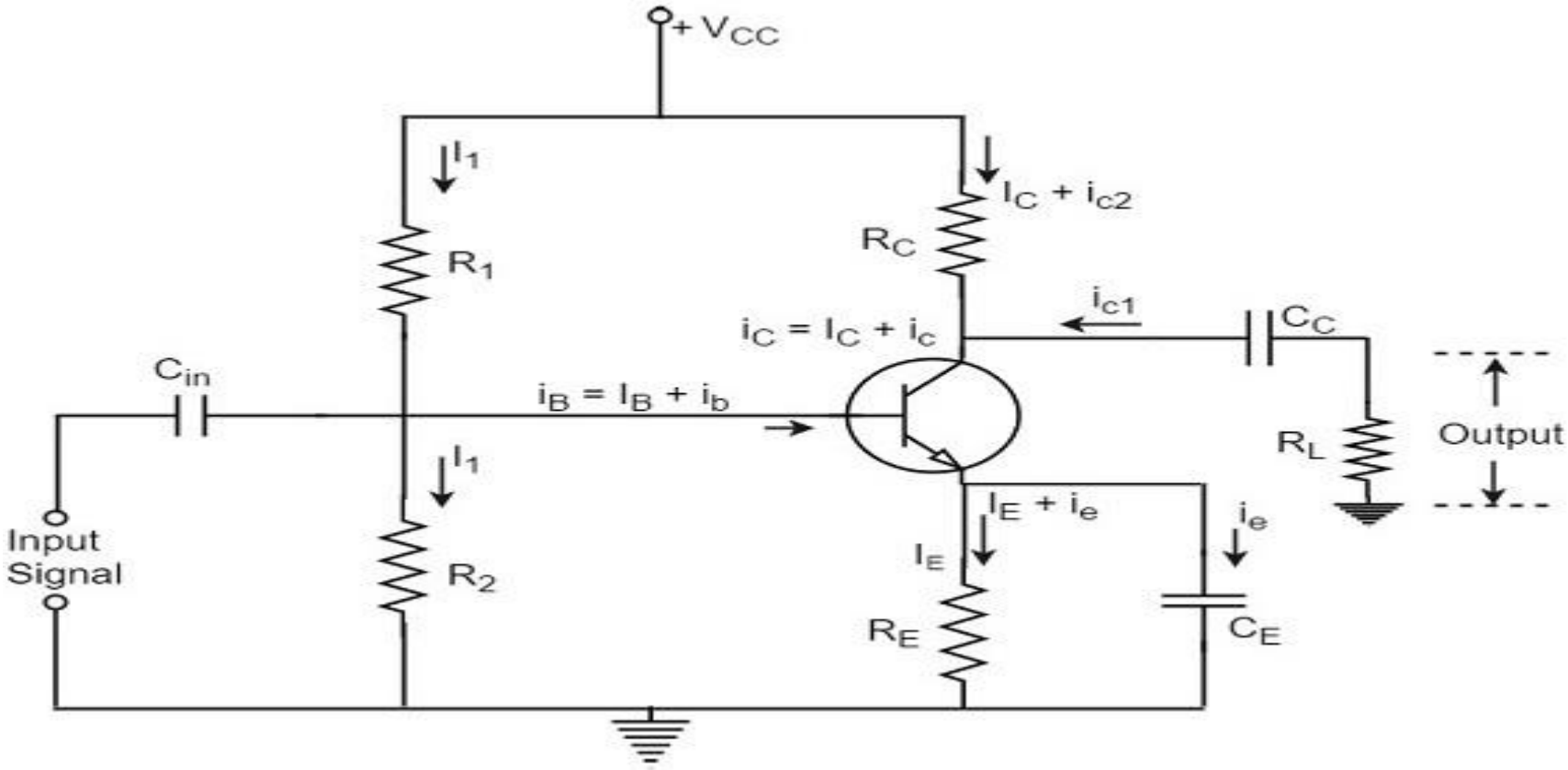
By definition, it is the ratio of output signal power to the input signal power.

$$\text{Power gain, } A_P = \frac{(\Delta I_C)^2 \times R_{AC}}{(\Delta I_B)^2 \times R_i}$$

$$= \left(\frac{\Delta I_C}{\Delta I_B}\right) \times \frac{\Delta I_C \times R_{AC}}{\Delta I_B \times R_i}$$

= Current gain × Voltage gain

CE Amplifier



CE Amplifier

Biasing Circuit

The resistors R_1, R_2 and R_E form the biasing and stabilization circuit, which helps in establishing a proper operating point.

Input Capacitor C_{in}

This capacitor couples the input signal to the base of the transistor. The input capacitor C_{in} allows AC signal, but isolates the signal source from R_2. If this capacitor is not present, the input signal gets directly applied, which changes the bias at R_2.

Coupling Capacitor C_C

This capacitor is present at the end of one stage and connects it to the other stage. As it couples two stages it is called as **coupling capacitor**. This capacitor blocks DC of one stage to enter the other but allows AC to pass. Hence it is also called as **blocking capacitor**.

Due to the presence of coupling capacitor C_C, the output across the resistor R_L is free from the collector's DC voltage. If this is not present, the bias conditions of the next stage will be drastically changed due to the shunting effect of R_C, as it would come in parallel to R_2 of the next stage.

Emitter by-pass capacitor C_E

This capacitor is employed in parallel to the emitter resistor R_E. The amplified AC signal is by passed through this. If this is not present, that signal will pass through R_E which produces a voltage drop across R_E that will feedback the input signal reducing the output voltage.

CE Amplifier

The Load resistor R_L

The resistance R_L connected at the output is known as **Load resistor**. When a number of stages are used, then R_L represents the input resistance of the next stage.

Various Circuit currents

Let us go through various circuit currents in the complete amplifier circuit. These are already mentioned in the above figure.

Base Current

When no signal is applied in the base circuit, DC base current I_B flows due to biasing circuit. When AC signal is applied, AC base current i_b also flows. Therefore, with the application of signal, total base current i_B is given by

$$i_B = I_B + i_b$$

Collector Current

When no signal is applied, a DC collector current I_C flows due to biasing circuit. When AC signal is applied, AC collector current i_c also flows. Therefore, the total collector current i_C is given by

$$i_C = I_C + i_c$$

Where

$I_C = \beta I_B$ = zero signal collecor current

$i_c = \beta i_b$ = collecor current due to signal

Emitter Current

When no signal is applied, a DC emitter current I_E flows. With the application of signal, total emitter current i_E is given by

$$i_E = I_E + i_e$$

It should be remembered that

$$I_E = I_B + I_C$$

$$i_e = i_b + i_c$$

As base current is usually small, it is to be noted that

$$I_E \cong I_C \quad \text{and} \quad i_e \cong i_c$$

Operation

- When no input is applied, the quiescent conditions are formed and no output is present. When positive half of the signal is being applied, the voltage between base and emitter V_{be} is increased because it is already positive with respect to ground.
- As forward bias increases, the base current too increases accordingly. Since $I_C = \beta I_B$, the collector current increases as well.

Operation

The collector current when flows through R_C, the voltage drop increases.

$$V_C = I_C R_C$$

As a consequence of this, the voltage between collector and emitter decreases. Because,

$$V_{CB} = V_{CC} - I_C R_C$$

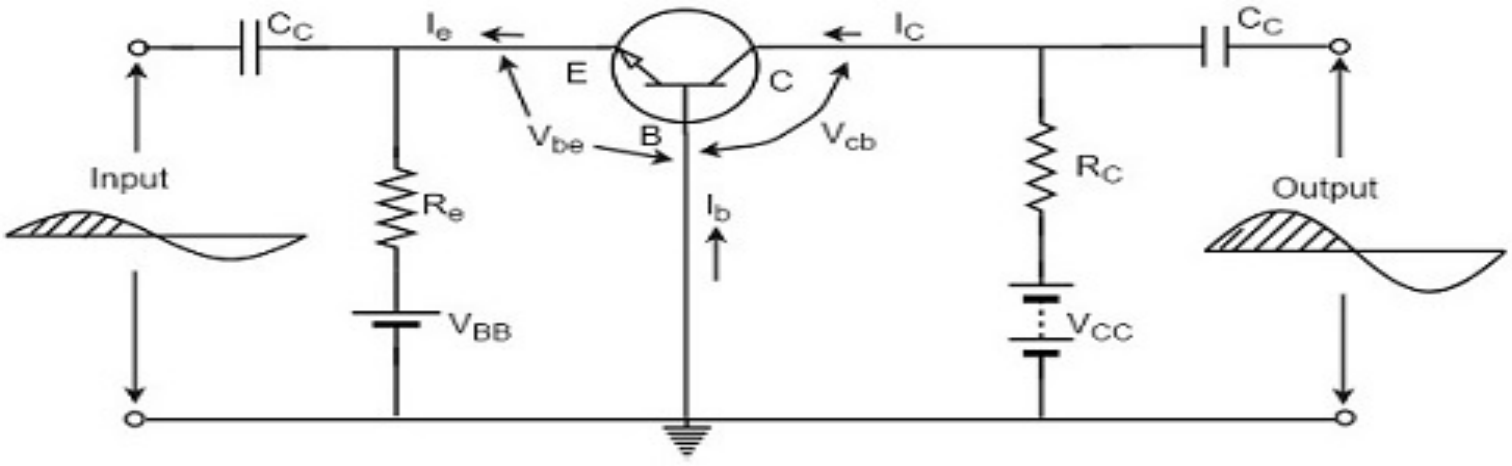
Thus, the amplified voltage appears across R_C.

Therefore, in a CE amplifier, as the positive going signal appears as a negative going signal, it is understood that there is a phase shift of 180^0 between input and output.

CE amplifier has a high input impedance and lower output impedance than CB amplifier. The voltage gain and power gain are also high in CE amplifier and hence this is mostly used in Audio amplifiers.

CB Amplifier

The input signal being applied at emitter base junction and the output signal being taken from collector base junction. The emitter base junction is forward biased by V_{EE} and collector base junction is reverse biased by V_{CC}. The operating point is adjusted with the help of resistors Re and R_c. Thus the values of I_c, I_b and I_{cb} are decided by V_{CC}, V_{EE}, R_e and R_c.



Operation

- When no input is applied, the quiescent conditions are formed and no output is present. As V_{be} is at negative with respect to ground, the forward bias is decreased, for the positive half of the input signal. As a result of this, the base current I_B also gets decreased.

Operation

As we know that,

$$I_C \cong I_E \cong \beta I_B$$

Both the collector current and emitter current get decreased.

The voltage drop across R_C is

$$V_C = I_C R_C$$

This V_C also gets decreased.

As $I_C R_C$ decreases, V_{CB} increases. It is because,

$$V_{CB} = V_{CC} - I_C R_C$$

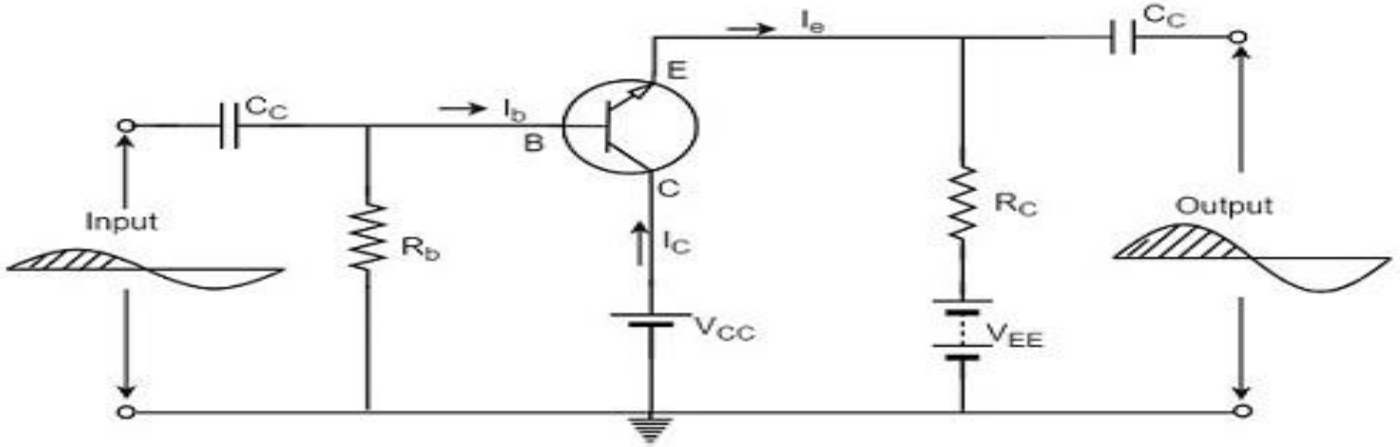
Thus, a positive half cycle output is produced.

In CB configuration, a positive input produces a positive output and hence input and output are in phase. So, there is no phase reversal between input and output in a CB amplifier.

If CB configuration is considered for amplification, it has low input impedance and high output impedance. The voltage gain is also low compared to CE configuration. Hence CB configured amplifiers are used at high frequency applications.

CC Amplifier

- The common collector amplifier circuit using NPN transistor is as shown below, the input signal being applied at base collector junction and the output signal being taken from emitter collector junction. The emitter base junction is forward biased by V_{EE} and collector base junction is reverse biased by V_{CC}. The Q-values of I_b and I_e are adjusted by R_b and R_e.



Operation

- When no input is applied, the quiescent conditions are formed and no output is present. When positive half of the signal is being applied, the forward bias is increased because V_{be} is positive with respect to collector or ground. With this, the base current I_B and the collector current I_C are increased. Consequently, the voltage drop across R_e i.e. the output voltage is increased. As a result, positive half cycle is obtained. As the input and output are in phase, there is no phase reversal.
- If CC configuration is considered for amplification, though CC amplifier has better input impedance and lower output impedance than CE amplifier, the voltage gain of CC is very less which limits its applications to impedance matching only.

Comparison between CB CE CC Amplifiers

Characteristic	CE	CB	CC
Input resistance	Low (1K to 2K)	Very low (30-150 Ω)	High (20-500 KΩ)
Output resistance	Large (≈ 50 K)	High (≈ 500 K)	Low (50-1000 KΩ)
Current gain	B high	$\alpha < 1$	High $(1 + \beta)$
Voltage gain	High (≈ 1500)	High (≈ 1500)	Less than one
Power gain	High (≈ 10,000)	High (≈ 7500)	Low (250-500)
Phase between input and output	reversed	same	same

Due to the compatibility and characteristic features, the common-emitter configuration is mostly used in amplifier circuits.

The Differential Amplifier

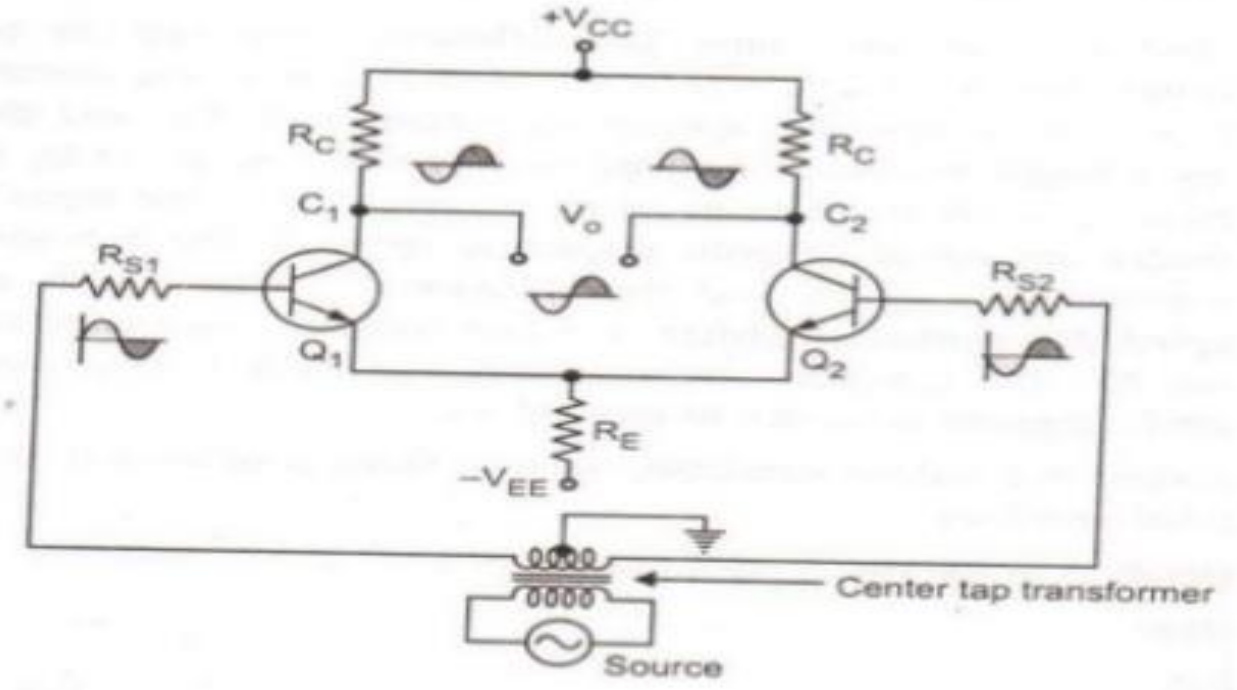
- An arrangement of transistors which allows the difference between two signals source to be amplified.
- The output is proportional to the difference between these two inputs.

Modes of operation of Differential Amplifier (DA)

- There are two modes of operations of DA
  - **Differential mode**
  - **Common mode**
- **Differential mode:**
  - Two input signals are of **same magnitude** but **opposite polarity** are used (180^0 out of phase)
- **Common mode**
  - Two input signals are of **equal in magnitude** and **same phase** are used

Differential mode

- Assume sine wave on base of Q1 is +ve going signal while on the base of Q2 –ve going signal



Differential mode

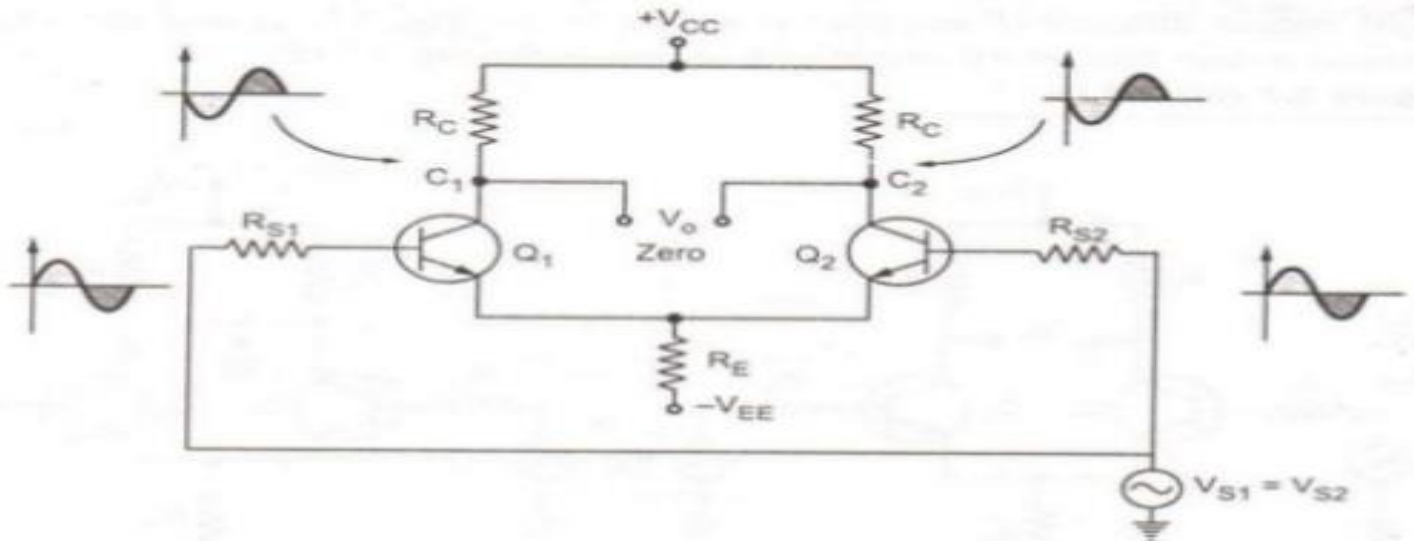
- An amplified –ve going signal will appear at collector of Q1
- An amplified +ve going signal will appear at collector of Q2
- Due to +ve going signal of base of Q1, current increases in R_E & hence a +ve going wave is developed across R_E
- Due to -ve going signal of base of Q2, -ve going wave is developed across R_E because of emitter follower action of Q2

Differential mode

- So, signal voltages across R_E, due to effect of Q1 &Q2 are equal in magnitude &180^0 out of phase- due to matched transistors
- Hence the two signals cancel each other & there is no signal across R_E
- No AC signal flows thro it
- V_o= +10-(-10)= 20
- V_o is difference voltage in two signals

Common Mode

- Two input signals are of equal in magnitude and same phase are used
- In phase signal develops in phase signal voltages across R_E



Common Mode

- Hence R_E carries a signal current & provides **-ve feedback**
- This –ve f/b decreases AC
- In signal voltages of equal magnitude will appear across two collectors of Q1 &Q2
- Vo= 10-10=0 Negligibly small
- Ideally it should be zero

CMRR

- The ability of a differential amplifier to reject a common mode signal is expressed by its common mode rejection ratio (CMRR)
- A high CMRR is required when a differential signal must be amplified in the presence of a possibly large common-mode input

CMRR

Common Mode Rejection Ratio

The ratio of the magnitude of its differential gain, A_d to the magnitude of its common mode gain, A_{CM}.

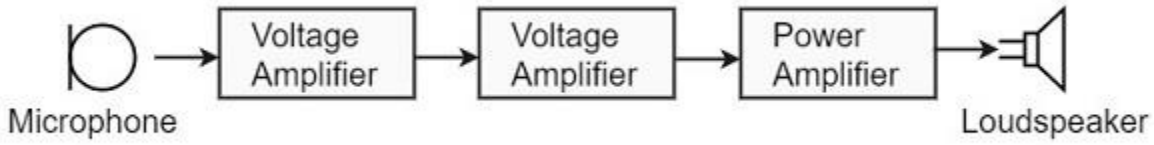
$$\text{CMRR} = \frac{|A_d|}{|A_{CM}|}$$

The value of the CMRR is often given in dB,

$$\text{CMRR (dB)} = 20 \log_{10} \frac{|A_d|}{|A_{CM}|}$$

Power Amplifier

- After the audio signal is converted into electrical signal, it has several voltage amplifications done, after which the power amplification of the amplified signal is done just before the loud speaker stage. This is clearly shown in the below figure.
-



Power Amplifier

- While the voltage amplifier raises the voltage level of the signal, the power amplifier raises the power level of the signal. Besides raising the power level, it can also be said that a power amplifier is a device which converts DC power to AC power and whose action is controlled by the input signal.
- The DC power is distributed according to the relation,
- DC power input = AC power output + losses

Power Transistor

- For such Power amplification, a normal transistor would not do. A transistor that is manufactured to suit the purpose of power amplification is called as a **Power transistor**.
- A Power transistor differs from the other transistors, in the following factors.
- It is larger in size, in order to handle large powers.
- The collector region of the transistor is made large and a heat sink is placed at the collector-base junction in order to minimize heat generated.
- The emitter and base regions of a power transistor are heavily doped.
- Due to the low input resistance, it requires low input power.
- Hence there is a lot of difference in voltage amplification and power amplification. So, let us now try to get into the details to understand the differences between a voltage amplifier and a power amplifier.

Classification of Power Amplifiers

- The Power amplifiers amplify the power level of the signal. This amplification is done in the last stage in audio applications. The applications related to radio frequencies employ radio power amplifiers. But the **operating point** of a transistor, plays a very important role in determining the efficiency of the amplifier. The **main classification** is done based on this mode of operation.
- The classification is done based on their frequencies and also based on their mode of operation.

Classification Based on Frequencies

- Power amplifiers are divided into two categories, based on the frequencies they handle. They are as follows.
- **Audio Power Amplifiers** − The audio power amplifiers raise the power level of signals that have audio frequency range (20 Hz to 20 KHz). They are also known as **Small signal power amplifiers**.
- **Radio Power Amplifiers** − Radio Power Amplifiers or tuned power amplifiers raise the power level of signals that have radio frequency range (3 KHz to 300 GHz). They are also known as **large signal power amplifiers**.

Classification Based on Mode of Operation

- On the basis of the mode of operation, i.e., the portion of the input cycle during which collector current flows, the power amplifiers may be classified as follows.
- **Class A Power amplifier** – When the collector current flows at all times during the full cycle of signal, the power amplifier is known as **class A power amplifier**.
- **Class B Power amplifier** – When the collector current flows only during the positive half cycle of the input signal, the power amplifier is known as **class B power amplifier**.
- **Class C Power amplifier** – When the collector current flows for less than half cycle of the input signal, the power amplifier is known as **class C power amplifier**.
- There forms another amplifier called Class AB amplifier, if we combine the class A and class B amplifiers so as to utilize the advantages of both.
- Before going into the details of these amplifiers, let us have a look at the important terms that have to be considered to determine the efficiency of an amplifier.

Collector Efficiency

- This explains how well an amplifier converts DC power to AC power. When the DC supply is given by the battery but no AC signal input is given, the collector output at such a condition is observed as **collector efficiency**.
- For example, if the battery supplies 15W and AC output power is 3W. Then the transistor efficiency will be 20%.
- The main aim of a power amplifier is to obtain maximum collector efficiency. Hence the higher the value of collector efficiency, the efficient the amplifier will be.

The collector efficiency is defined as

$$\eta = \frac{average\ a.c\ power\ output}{average\ d.c\ power\ input\ to\ transistor}$$

Power Dissipation Capacity

- Every transistor gets heated up during its operation. As a power transistor handles large currents, it gets more heated up. This heat increases the temperature of the transistor, which alters the operating point of the transistor.
- So, in order to maintain the operating point stability, the temperature of the transistor has to be kept in permissible limits. For this, the heat produced has to be dissipated. Such a capacity is called as Power dissipation capability.
- **Power dissipation capability** can be defined as the ability of a power transistor to dissipate the heat developed in it. Metal cases called heat sinks are used in order to dissipate the heat produced in power transistors.

Distortion

- A transistor is a non-linear device. When compared with the input, there occur few variations in the output. In voltage amplifiers, this problem is not pre-dominant as small currents are used. But in power amplifiers, as large currents are in use, the problem of distortion certainly arises.
- **Distortion** is defined as the change of output wave shape from the input wave shape of the amplifier. An amplifier that has lesser distortion, produces a better output and hence considered efficient.

Power Amplifier

Amplifier Types

Class A

The amplifier conducts through the full 360° of the input. The Q-point is set near the middle of the load line.

Class B

The amplifier conducts through 180° of the input. The Q-point is set at the cutoff point.

Class AB

This is a compromise between the class A and B amplifiers. The amplifier conducts somewhere between 180° and 360° . The Q-point is located between the mid-point and cutoff.

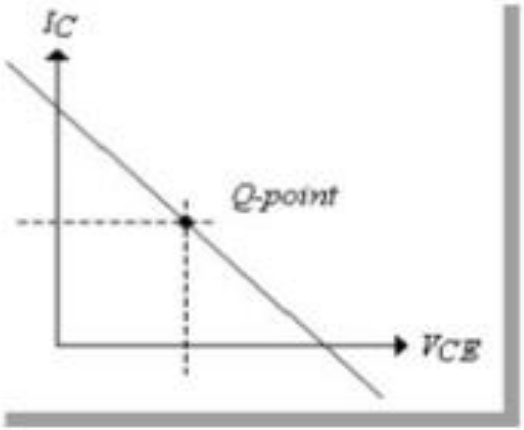
Class C

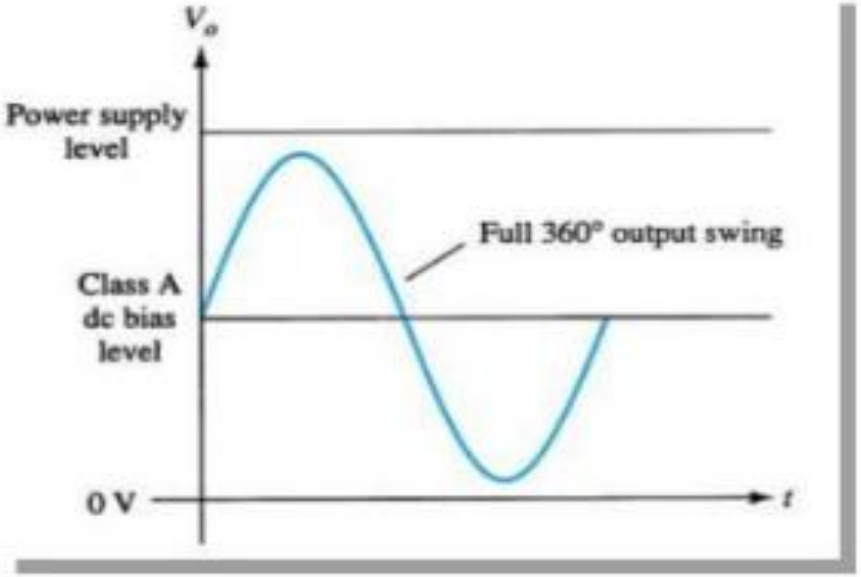
The amplifier conducts less than 180 of the input. The Q-point is located below the cutoff level.

Class A Amplifier

The output of a class A amplifier conducts for the full 360° of the cycle.

The Q-point is set at the middle of the load line so that the AC signal can swing a full cycle.

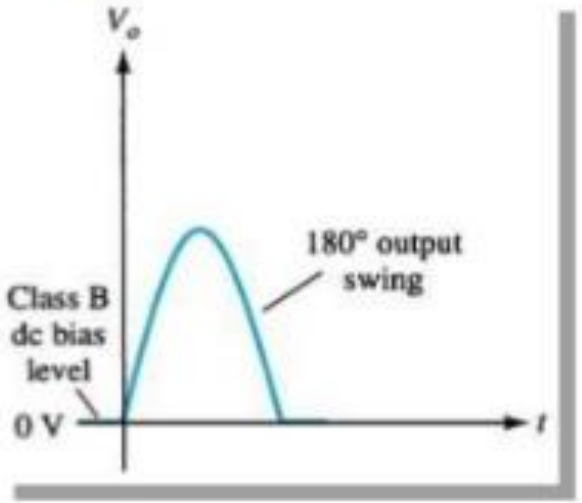


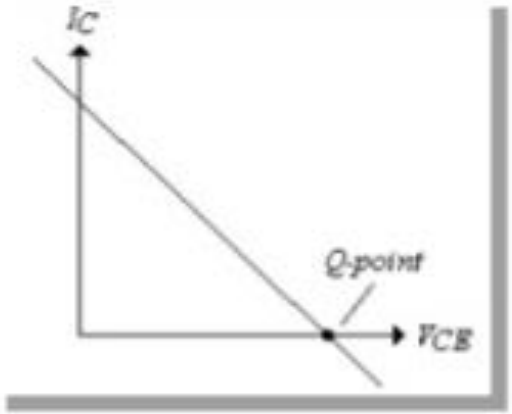


Remember that the DC load line indicates the maximum and minimum limits set by the DC power supply.

Class B Amplifier

A class B amplifier output only conducts for 180° or one-half of the AC input signal.

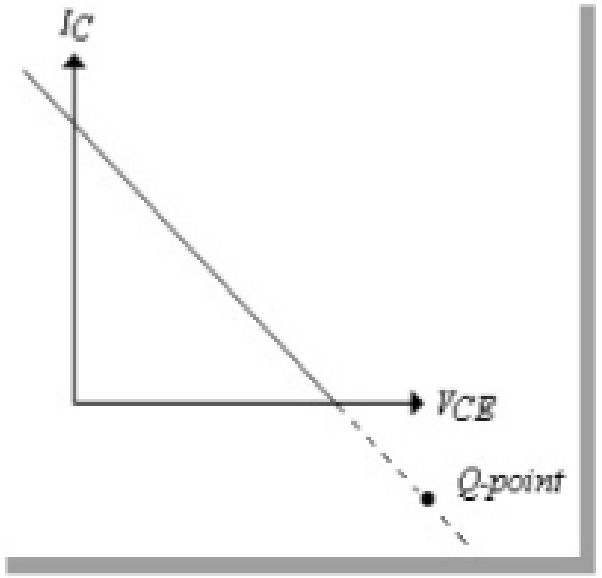




The Q-point is at 0V on the load line, so that the AC signal can only swing for one-half cycle.

Class C

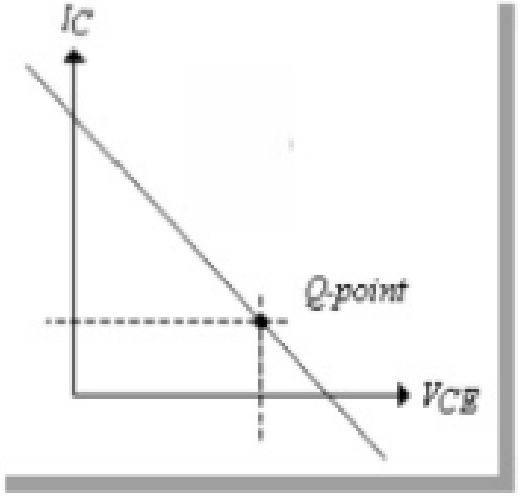
The output of the class C conducts for less than 180° of the AC cycle. The Q-point is below cutoff.



Class AB Amplifier

This amplifier is a compromise between the class A and class B amplifier—the Q-point is above that of the Class B but below the class A.

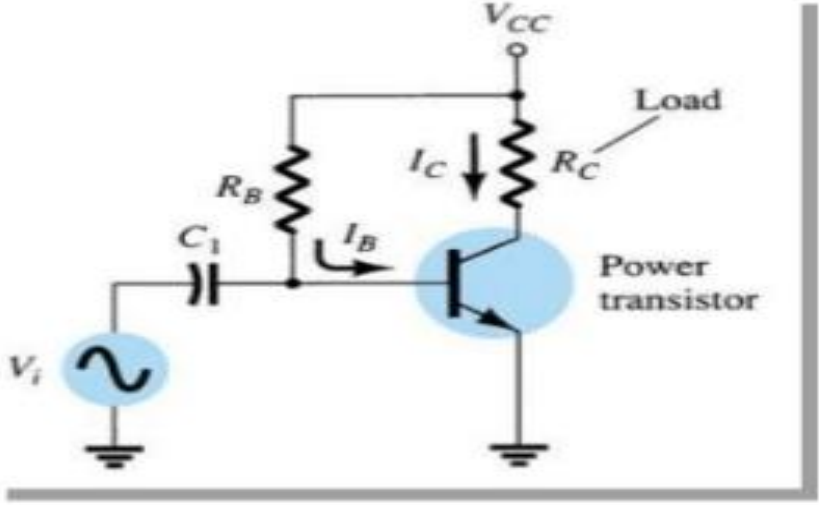
The output conducts between 180° and 360° of the AC input signal.



Direct coupled class A amplifier

Series-Fed Class A Amplifier

This is similar to the small-signal amplifier except that it will handle higher voltages. The transistor used is a high-power transistor.



Power Considerations

- The power drawn from the supply is $P_i(\text{dc}) = V_{CC} I_{C_Q}$

- Output Power

$$P_o(\text{ac}) = V_{CE}(\text{rms}) I_C(\text{rms})$$

$$P_o(\text{ac}) = I_C^2(\text{rms}) R_C$$

$$P_o(\text{ac}) = \frac{V_C^2(\text{rms})}{R_C}$$

- Efficiency

$$\% \, \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\%$$

- Maximum Efficiency

$$\text{maximum } V_{CE}(\text{p-p}) = V_{CC}$$

$$\text{maximum } I_C(\text{p-p}) = \frac{V_{CC}}{R_C}$$

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}(V_{CC}/R_C)}{8} = \frac{V_{CC}^2}{8R_C}$$

$$\text{maximum } P_i(\text{dc}) = V_{CC}(\text{maximum } I_C) = V_{CC}\frac{V_{CC}/R_C}{2} = \frac{V_{CC}^2}{2R_C}$$

The maximum power input can be calculated using the dc bias current set to one-half the

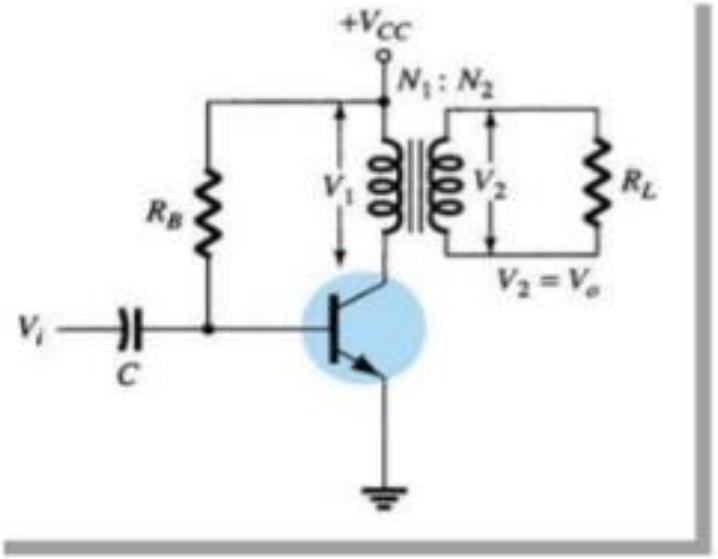
$$\text{maximum } \% \, \eta = \frac{\text{maximum } P_o(\text{ac})}{\text{maximum } P_i(\text{dc})} \times 100\% = \frac{V_{CC}^2/8R_C}{V_{CC}^2/2R_C} \times 100\% = 25\%$$

N.B.:

$$V_{\text{RMS}} = \frac{V_{\text{p}}}{\sqrt{2}}$$

Transformer-Coupled Class A Amplifier

This circuit uses a transformer to couple to the load. This improves the efficiency of the Class A to 50%.

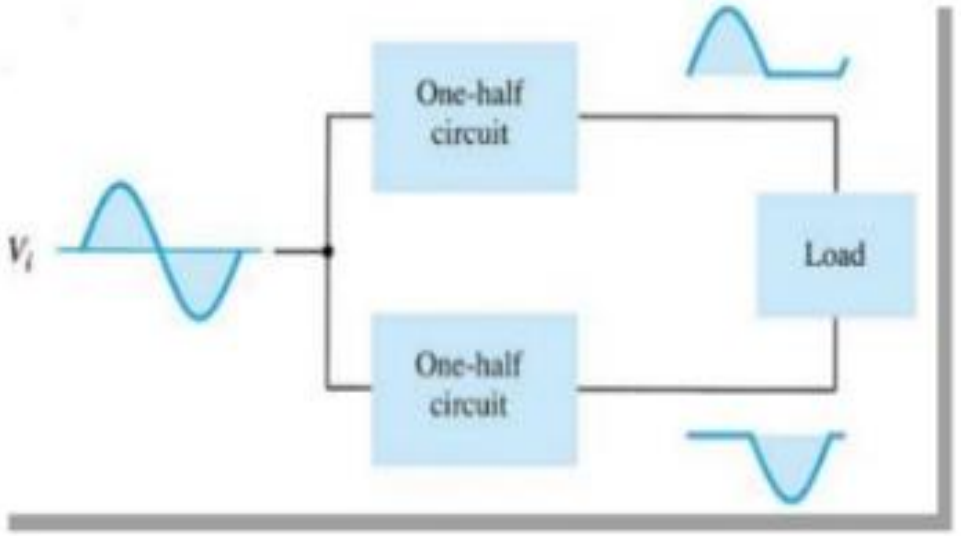


Class B Amplifier

In class B, the transistor is biased just off. The AC signal turns the transistor on.

The transistor only conducts when it is turned on by one-half of the AC cycle.

In order to get a full AC cycle out of a class B amplifier, you need two transistors:



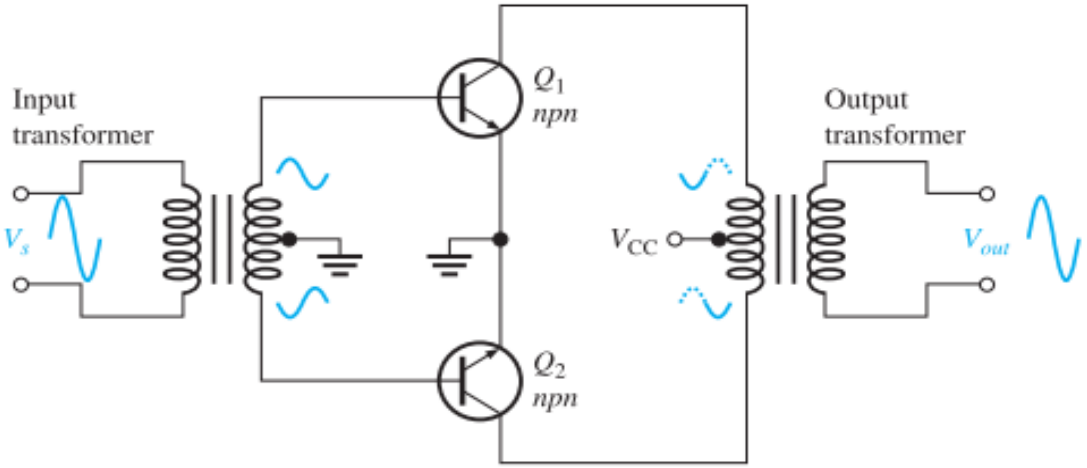
- An *npn* transistor that provides the negative half of the AC cycle
- A *pnp* transistor that provides the positive half.

Class B Push-Pull Operation

- To amplify the entire cycle, it is necessary to add a second class B amplifier that operates on the negative half of the cycle.
- The combination of two class B amplifiers working together is called push-pull operation
- There are **two common approaches** for using push-pull amplifiers to reproduce the entire waveform.

1. Transformer Coupling

- ✓ The input transformer thus converts the input signal to two out-of-phase signals for the two npn transistors.



- ✓ The output transformer combines the signals by permitting current in both directions, even though one transistor is always cut off.

Maximum Output Power

$$P_{out} = I_{out(rms)} V_{out(rms)}$$

$$P_{out} = 0.5 I_{c(sat)} V_{CEQ}$$

$$I_{out(rms)} = 0.707 I_{out(peak)} = 0.707 I_{c(sat)}$$

$$V_{out(rms)} = 0.707 V_{out(peak)} = 0.707 V_{CEQ}$$

Substituting $V_{CC}/2$ for V_{CEQ}, the maximum average output power is

$$\boldsymbol{P_{out} = 0.25 I_{c(sat)} V_{CC}}$$

DC Input Power

The dc input power comes from the V_{CC} supply and is

$$P_{DC} = I_{CC} V_{CC}$$

Since each transistor draws current for a half-cycle, the current is a half-wave signal with an average value of

$$I_{CC} = \frac{I_{c(sat)}}{\pi}$$

$$P_{DC} = \frac{I_{c(sat)} V_{CC}}{\pi}$$

Efficiency

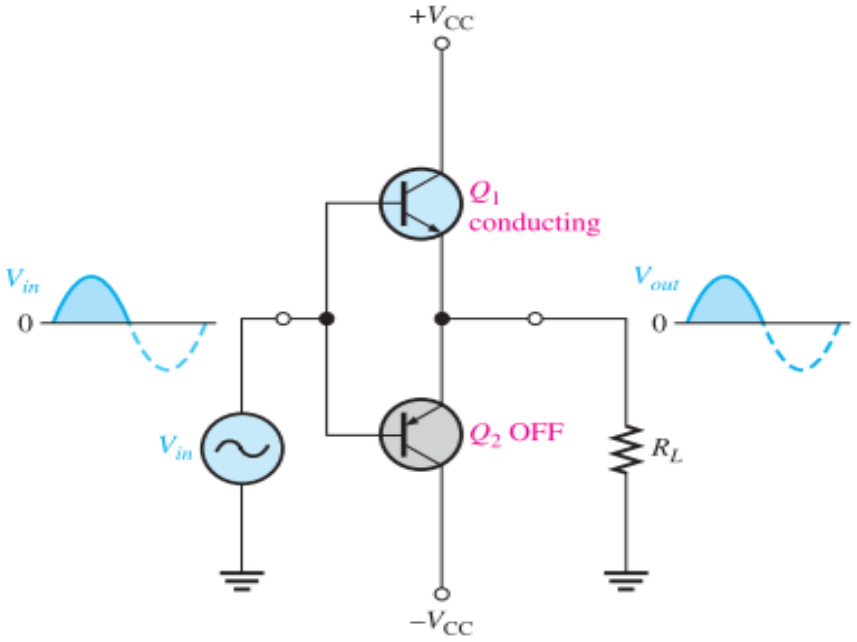
$$\eta = \frac{P_{out}}{P_{DC}}$$

$$\eta_{max} = \frac{P_{out}}{P_{DC}} = \frac{0.25 I_{c(sat)} V_{CC}}{I_{c(sat)} V_{CC}/\pi} = 0.25\pi$$

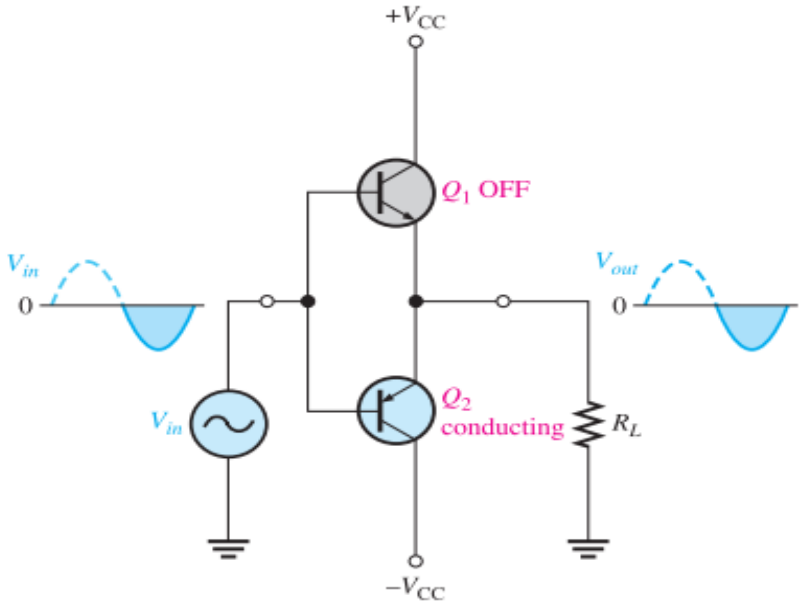
$$\boldsymbol{\eta_{max} = 0.79}$$

2. Complementary Symmetry Transistors

- ✓ The figure shows one of the most popular types of push-pull class B amplifiers using two emitter-followers and both positive and negative power supplies.
- ✓ This is a complementary amplifier because one emitter-follower uses an npn transistor and the other a pnp, which conduct on opposite alternations of the input cycle.



(a) During a positive half-cycle

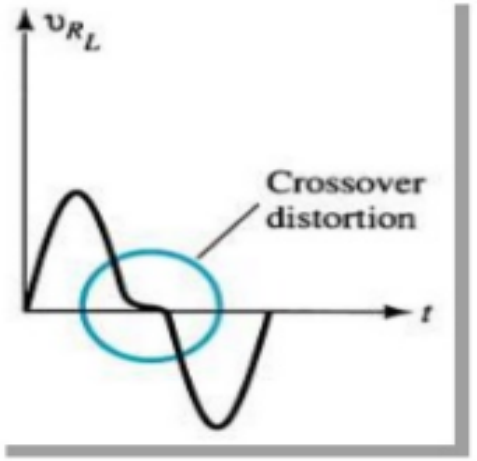


(b) During a negative half-cycle

Class B Amplifier

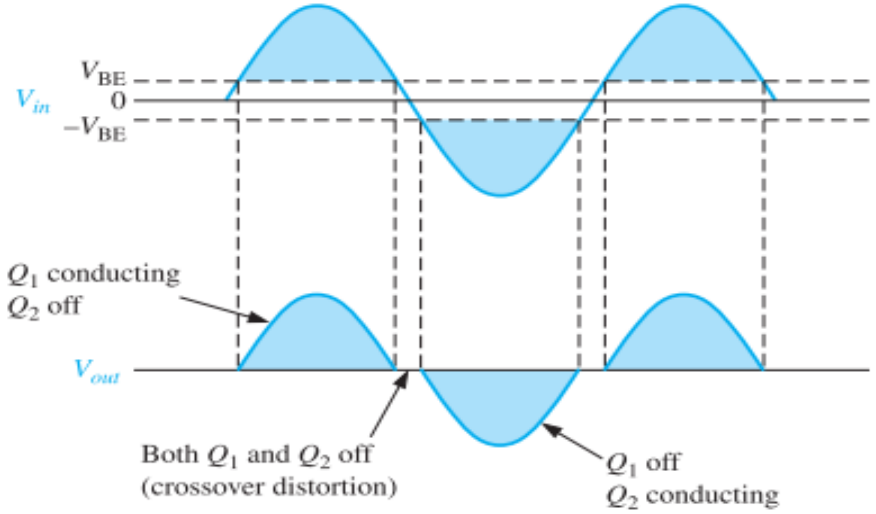
Crossover Distortion

If the transistors Q_1 and Q_2 do not turn on and off at exactly the same time, then there is a gap in the output voltage.



Crossover Distortion

- ✓ When the dc base voltage is zero, both transistors are off and the input signal voltage must exceed V_{BE} before a transistor conducts.
- ✓ Because of this, there is a time interval between the positive and negative alternations of the input when neither transistor is conducting, as shown in Figure.
- ✓ The resulting distortion in the output waveform is called **crossover distortion**.



Multistage Amplifier

MULTISTAGE TRANSISTOR AMPLIFIER

A transistor circuit containing more than one stage of amplification is known as **multistage transistor amplifier.**

Fig: Block diagram of a 3-stage amplifier

In a multistage amplifier, a number of single amplifiers are connected.

Multi-Stage Transistor Amplifier

- In Multi-stage amplifiers, the output of first stage is coupled to the input of next stage using a coupling device. These coupling devices can usually be a capacitor or a transformer. This process of joining two amplifier stages using a coupling device can be called as **Cascading**.

- The following figure shows a two-stage amplifier connected in cascade.
- *The overall gain is the product of voltage gain of* individual stages.

$$A_V = A_{V1} \times A_{V2} = \frac{V_2}{V_1} \times \frac{V_0}{V_2} = \frac{V_0}{V_1}$$

- Where A_V = Overall gain, A_{V1} = Voltage gain of 1st stage, and A_{V2} = Voltage gain of 2nd stage.
- If there are **n** number of stages, the product of voltage gains of those **n** stages will be the overall gain of that multistage amplifier circuit.
-

Purpose of coupling device

- The basic purposes of a coupling device are
- To transfer the AC from the output of one stage to the input of next stage.
- To block the DC to pass from the output of one stage to the input of next stage, which means to isolate the DC conditions.

Resistance-Capacitance Coupling

- This is the mostly used method of coupling, formed using simple **resistor-capacitor** combination. The capacitor which allows AC and blocks DC is the main coupling element used here.
- The coupling capacitor passes the AC from the output of one stage to the input of its next stage. While blocking the DC components from DC bias voltages to effect the next stage.

Impedance Coupling

- The coupling network that uses **inductance** and **capacitance** as coupling elements can be called as Impedance coupling network.
- In this impedance coupling method, the impedance of coupling coil depends on its inductance and signal frequency which is **jwL**. This method is not so popular and is seldom employed.

Transformer Coupling

- The coupling method that uses a **transformer as the coupling** device can be called as Transformer coupling. There is no capacitor used in this method of coupling because the transformer itself conveys the AC component directly to the base of second stage.
- The secondary winding of the transformer provides a base return path and hence there is no need of base resistance. This coupling is popular for its efficiency and its impedance matching and hence it is mostly used.

Direct Coupling

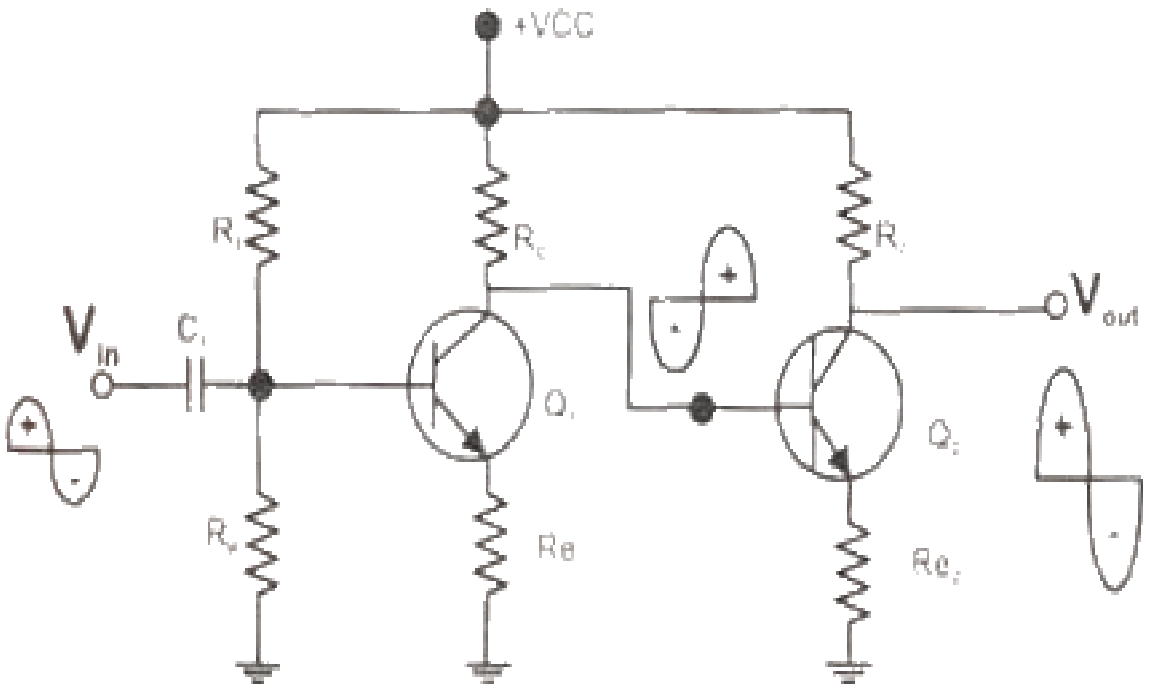
- If the previous amplifier stage is connected to the next amplifier stage directly, it is called as **direct coupling**. The individual amplifier stage bias conditions are so designed that the stages can be directly connected without DC isolation.
- The direct coupling method is mostly used when the load is connected in series, with the output terminal of the active circuit element. For example, head-phones, loud speakers etc.

Direct Coupled Amplifier

As shown in the below diagram, the direct coupled amplifier (DC) is consist of two transistors Q_1 and Q_2 , a voltage divider base bias resistor network (R_1, R_2) which is provided on the transistor Q_1 base

two collector resistors $R_{C1}$and R_{C2}, the transistor Q_2 is self biased, we also use tow emitter bypass resistors $R_{E1}$and R_{E2}. The direct-coupled amplifier is operated without the using of frequency sensitive component like capacitor, inductor and Transformer etc. The direct coupled amplifier amplify the A.C signal with frequency as low a fraction of Hertz (Hz).

Direct Coupled Amplifier



Direct Coupled Amplifier

Direct Coupled Amplifier

First of all when we applied a +ve half cycle at the I/P of Q_1 transistor, which is already biased through the divider bias network. The +ve half cycle forwarded bias the transistor Q_1 which start the conduction and give an inverted and amplified O/P at the collector . As we know that,

$V_{CE} = V_{cc} - I_c R_c$

This amplified -ve signed is provided to the base of Q_2 transistor, which is self-bias (because they are connected in cascade condition). The base of Q_2 transistor is a reversed and did not conduct, the O/P of transistor Q_2 is amplified signal (inverting to I/P of Q_2) when the Q_2 did not conduct and the voltage drop across collector emitter will be zero, therefore the V_{CC} is equal to $I_c R_c$.

Direct Coupled Amplifier

- The transistor in the first stage will be an NPN transistor, while the transistor in the next stage will be a PNP transistor and so on. This is because, the variations in one transistor tend to cancel the variations in the other. The rise in the collector current and the variation in β of one transistor gets cancelled by the decrease in the other.

Direct Coupled Amplifier

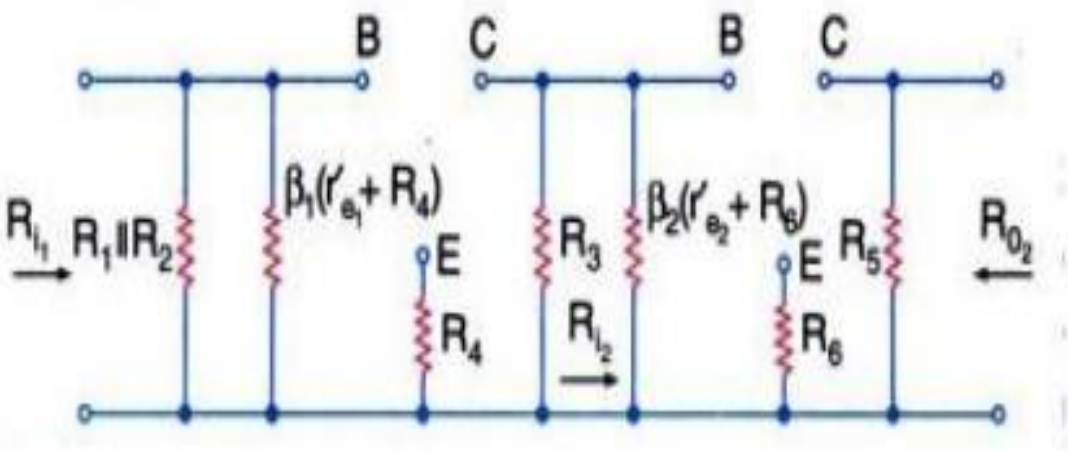
Operation

- The input signal when applied at the base of transistor T_1, it gets amplified due to the transistor action and the amplified output appears at the collector resistor R_c of transistor T_1. This output is applied to the base of transistor T_2which further amplifies the signal. In this way, a signal is amplified in a direct coupled amplifier circuit.

Direct Coupled Amplifier

4-1 calculation of Voltage Gain of Direct Coupled Amplifier:

Consider Fig.(1-9).



Direct Coupled Amplifier

It is evident from the figure shown above that the input resistance of the first stage,

$$R_{i_1} = (R_1 \parallel R_2) \parallel \beta_1 (r'_{e_1} + R_4)$$

and input resistance of the second stage,

$$R_{i_2} = \beta_2 (r'_{e_2} + R_6)$$

Similarly, the output resistance of the first stage,

$$R_{o_1} = R_3 \parallel R_{i_2}$$

and output resistance of the second stage,

$$R_{o_2} = R_5$$

$\therefore$ Voltage gain of the first stage,

$$A_{v_1} = \beta \times \frac{R_{o_1}}{R_{i_1}} = \frac{R_{o_1}}{r'_{e1} + R_4}$$

and voltage gain of the second stage,

$$A_{v_2} = \beta_2 \times \frac{R_{o_2}}{R_{i_2}} = \frac{R_{o_2}}{r'_{e_2} + R_4}$$

Now the overall voltage gain is given by the relation,

$$A_v = A_{v_1} \cdot A_{v_2}$$

18·12. MOSFETs

The MOSFET is an abbreviation for metal-oxide semiconductor field-effect transistor. Like JFET, it has a source, gate and drain. However, unlike JFET, the gate of a MOSFET is insulated from the channel. Because of this, the MOSFET is sometimes known as an IGFET which stands for insulated-gate field effect transistor. Basically, the MOFET's are of two types namely depletion type MOSFET and Enhance-type MOSFET.

18·13. Depletion-type MOSFET

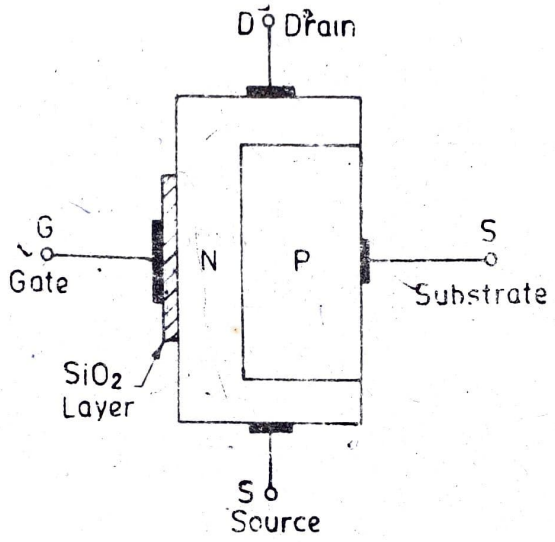


Fig. 18·11· Basic structure of an N-channel depletion-type MOSFET.

Fig. 18·11 shows the basic structure of an N-channel depletion type MOSFET. It consists of a conducting bar of N-type material with an insulated gate on the left and P-region on the right. Free electrons can flow from source to drain through the N-type material. The P-region is called substrate (or body). It physically reduces the conducting path to a narrow channel. A thin layer of silicon dioxide is deposited on the left side of the channel. This layer insulates the gate from the channel. Because of this, a negligible gate current flows even when the gate voltage is positive. It will be interesting to know that a PN juction, which exists in a JFET, has been eliminated in the MOSFET.

The basic construction of a depletion-type P-channel MOSFET is similar to that of N-channel except that the conducting bar is of P-type material and the substrate is of N-type material.

18·14. Working of a Depletion-type MOSFET

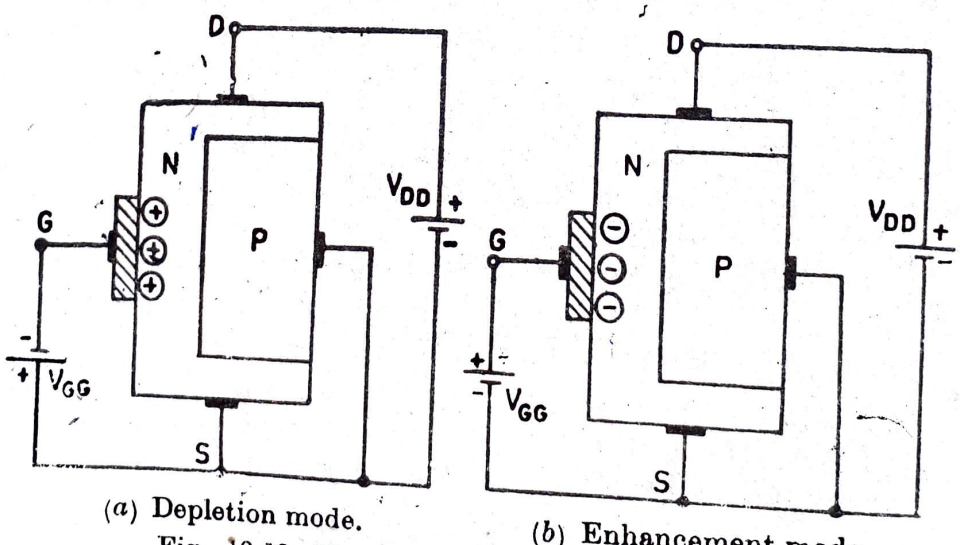
The depletion-type MOSFET can be operated in two different modes as given below :

1. *Depletion mode.* The device operates in this mode, when the gate voltage is negative.
2. *Enhancement mode.* The device operates in this mode, when the gate voltage is positive.

Since the depletion-type MOSFET can be operated in either depletion or enhancement mode, therefore this device is commonly known as depletion-enhancement (DE) type MOSFET. The working of a MOSFET may by explained easily, if we visulise the entire structure of the device as a parallel plate capacitor. One of the plates is formed by the gate and the other by the semiconductor channel. The plates are separated by a dielectric (SiO_2 layer). We know that if one plate of a capacitor is made negative, it induces a positive charge on the opposite plate and vice versa. This principle is used below in explaining the working of MOSFET's in the depletion and enhancement modes.

1. *Depletion mode.* Fig. 18·12 (*a*) shows a MOSFET with a negative gate-to-source voltage. The negative voltage, on the gate, induces a positive charge in the channel. Because of this, free electrons in the vicinity of positive charge are repelled away in the channel. As a result of this, the channel is depleted of free electrons. This reduces the number of free electrons (which constitute the drain current) passing through the channel. Thus as the value of negative gate-to-source voltage is increased, the value of drain current decreases. At a sufficient negative value of gate-to-source voltage, called V_{GS} (off), the channel is totally depleted of free electrons and therefore the drain current reduces to zero. Thus with the negative gate voltage, the operation of MOSFET is similar to that of a JFET.

It is evident from the above discussion that negative gate voltage depletes the channel of free electrons. It is due to this fact that the working of a MOSFET, with a negative gate voltage, is called depletion mode.



(*a*) Depletion mode. (*b*) Enhancement mode.

Fig. 18·12. Working of a depletion-type MOSFET.

2. *Enhanbement mode.* Fig. 18 12 (*b*) shows a MOSFET with a positive gate-to-source voltage. The positive gate voltage increases the number of free electrons passing through the channel. The greater the gate voltage, greater is the number of free electrons passing through the channel. This increases i.e. enhances the conducting of the channel. Because of this fact, positive gate operation is called enhancement mode.

It will be interesting to know that depletion-type MOSFET can conduct even if the gate-to-source voltage (V_{GS}) is zero. Because of this, it is commonly known as Normally-ON MOSFET.

18·15. Drain Characteristic of Depletion-type MOSFET

Fig. 18·13 shows the drain characteristics for the N-channel depletion-type MOSFET in the common source configuration. These curves are plotted for both negative and positive values of gate-to-source voltage (V_{GS}). The curves shown above the curve for $V_{GS}=0$ have a positive zero whereas those below it have a negative value of V_{GS}. When V_{GS} is zero and negative, the MOSFET operates in the depletion-mode. On the other hand, if V_{GS} is zero and positive, the MOSFET operates in the enhancement-mode.

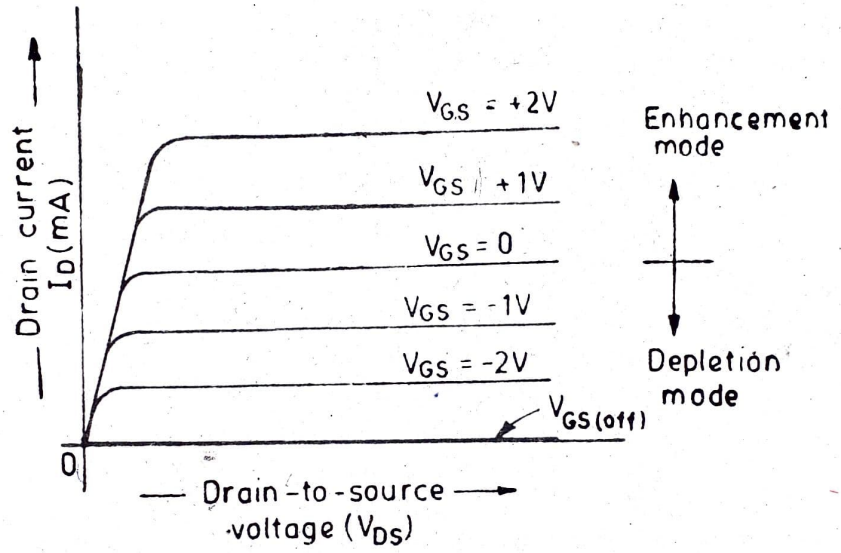


Fig. 18·13. Drain characteristics of N-channel depletion-type MOSFET.

It may be noted that the drain characteristics of depletion-type MOSFET's are similar to that of JFET. The only difference is that JFET does not operate for positive values of gate-to-source voltage (V_{GS}).

18·16. Transfer Characteristic of Depletion-type MOSFET

Fig. 18·14 shows the transfer characteristic (also called transconductance curve) for an N-channel depletion-type MOSFET. It may be noted from this curve that the region AB of the characteristic is similar to that of JFET. But here, this curve extends for the positive values of gate-to-source voltage (V_{GS}) also. The value I_{DSS} represents the current from drain-to-source with $V_{GS} = 0$. The drain current at any point along the transfer characteristic (*i.e.* the curve ABC) is given by the relation,

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2$$

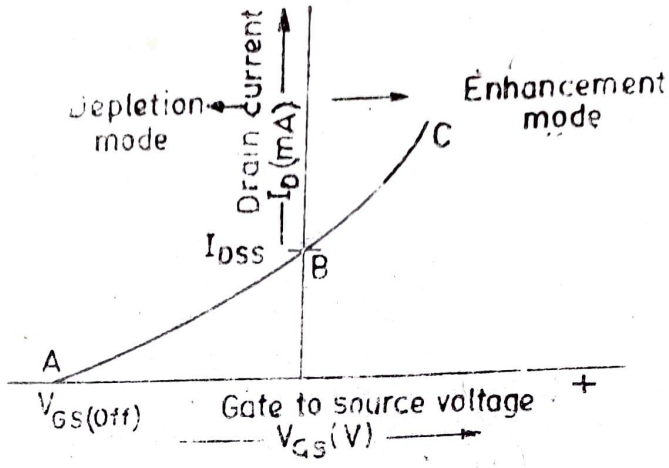
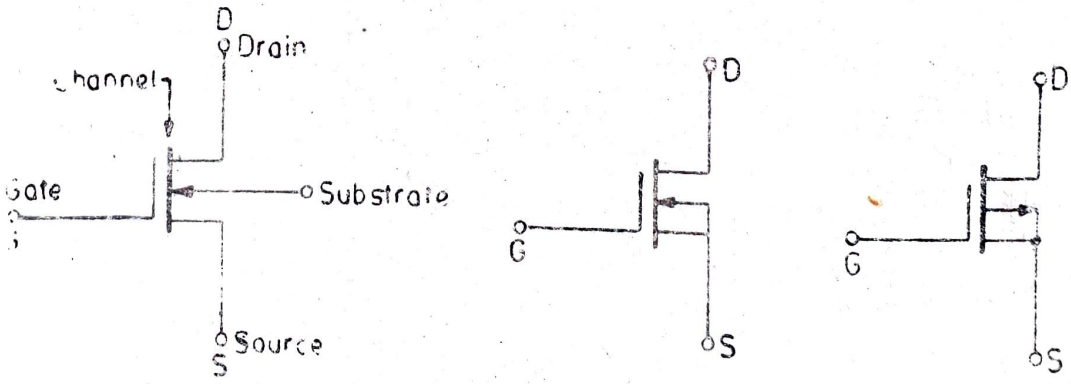


Fig. 18·14. Transfer characteristics of a N-channel depletion-type MOSFET.

It may be noted that even if $V_{GS} = 0$, the device has a drain current equal to I_{DSS}. Due to this fact, it is called normally-ON MOSFET.

18·17. Circuit Symbol for Depletion-type MOSFET

Fig. 18·15 (*a*) and (*b*) shows the circuit symbols for the N-channel depletion-type MOSFET. In these figures, a thin vertical line (just right to the gate) represents the channel. The drain and source terminals are connected to the top and bottom of the channel as shown. The arrow, on the P-type substrate, points towards the channel. This indicates that the channel is N-type. In some MOSFET's, a connection from the substrate is also taken out. Such MOSFET's have 4-terminals as indicated in the Fig. 18·15 (*a*). But in most of the MOSFET's the substrate is internally connected to the source. This results in a three terminal device, whose circuit symbol is as shown in Fig. 18·15 (*b*).



(*a*) N-channel (*b*) N-channel (*c*) P-channel

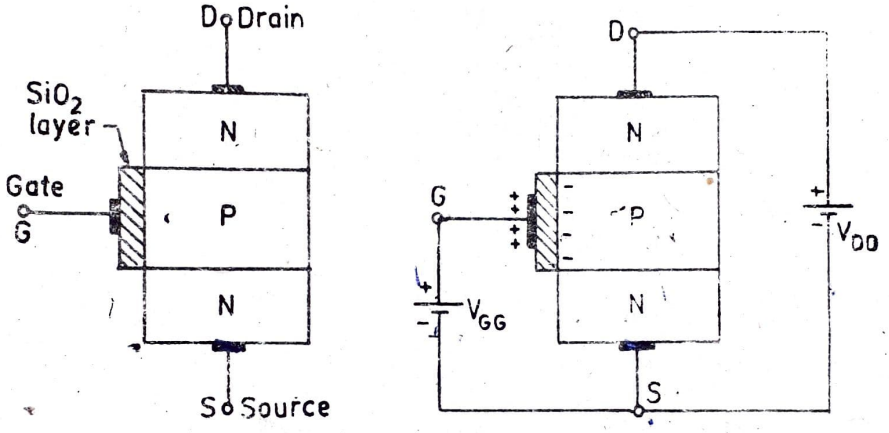
Fig. 18·15. Circuit symbols for depletion type MOSFET's,

Fig. 18·15 (*c*) shows the circuit symbol for a P-channel depletion type MOSFET. It may be noted that the symbol is similar to that of N-channel, except the direction of the arrow on the substrate. Its direction is away from the channel, which indicates that the channel is of P-type material.

18·18. Enhancement-type MOSFET

The enhancement-type MOSFET has no depletion mode and it operates only in enhancement mode. It differs in construction from the depletion-type MOSFET in the sense that it has no physical channel. Fig. 18·16 (*a*) shows the basic structure of the N-channel enhancement-type MOSFET. It may be noted, that the P-type substrate extends the silicon dioxide layer completely.

Fig. 18·16 (*b*) shows the normal biasing polarities for the N-channel enhancement-type MOSFET. It must be remembered that this MOSFET is always operated with the positive gate-to-source voltage (V_{GS}). When the gate-to-source voltage is zero, the V_{DD} supply tries to force free electrons from source-to-drain. But the presence of P-region does not permit the electrons to pass through it. Thus there is no drain current for $V_{GS} = 0$. Due to this fact, the enhancement type MOSFET is also called normally-OFF MOSFET.



(*a*) Basic construction. (*b*) Formation of invertion layer.

Fig. 18·16. Enhancement type MOSFET.

Now, if some positive voltage is applied at the gate, it induces a negative charge in the P-type substrate just adjacent to the silicon dioxide layer. The induced negative charge is produced by attracting the free electrons from the source. When the gate is positive enough, it can attract a number of free electrons. This forms a thin layer of electrons, which stretches from source to drain. This effect is equivalent to producing a thin layer of N-type channel in the P-type substrate. This layer of free electrons is called N-type invertion layer.

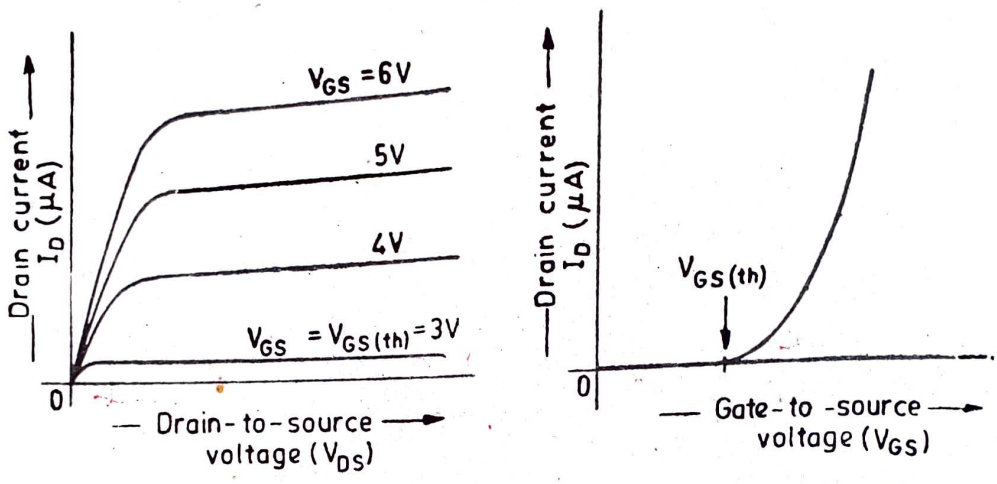
The minimum gate-to-source voltage (V_{GS}), which produces invertion layer, is called threshold voltage and is designated by the symbol $V_{GS(th)}$. When the voltage V_{GS} is less than $V_{GS(th)}$, no current flows from drain to source. However, when the voltage V_{GS} is greater than $V_{GS(th)}$, the inversion layer connects the drain and source and we get significant value of current.

18·19. Drain Characteristics for Enhancement-type MOSFET

Fig. 18·17 (*a*) shows the drain characteristics for N-channel enhancement-type MOSFET. It may be noted from this figure, that the gate-to-source voltage (V_{GS}) is less than threshold voltage,

$V_{GS(th)}$, there is no drain current. However, in actual practice, an extremely small value of drain current does flow through the MOSFET. This current flow is due to the presence of thermally generated electrons in the P-type substrate. When the value of V_{GS} is kept above $V_{GS(th)}$, a significant drain current flows.

The value of drain current increases with the increase in gate-to-source voltage. It is because of the fact that the width of inversion layer widens for increased value of V_{GS} and therefore allows more number of free electrons to pass through it. The drain current reaches its saturation value above a certain value of drain-to-source voltage (V_{DS}).



(*a*) Drain characteristic. (*b*) Transfer characteristic.

Fig. 18·17. Characteristics for N-channel enhancement-type MOSFET.

18·20. Transfer Characteristic for Enhancement-type MOSFET

Fig. 18·17 (*b*) shows the transfer characteristic for N-channel enhancement type MOSFET. It may be noted from this figure that there is no drain current when the gate-to-source voltage, $V_{GS} = 0$. However, if V_{GS} is increased above the threshold voltage, $V_{GS(th)}$, the drain current increases rapidly as shown in figure. The drain current at any point along the curve is given by the relation,

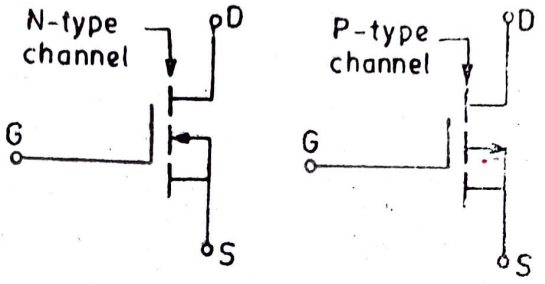
$$I_D = K\,[V_{GS} - V_{GS(th)}]^2$$

where K is a constant, whose value depends on the type of MOSFET. Its value can be determined from the data sheet by taking specified value of drain current called $I_{D(ON)}$ at the given value of V_{GS} and then substituting these values in the above equation. Incidently, it may be noted that enhancement-type MOSFET does not have an I_{DSS} perameter like JFET and depletion-type MOSFET.

18·21. Circuit Symbol for Enhancement-type MOSFET

Fig. 18·18 (*a*) shows the circuit symbol for N-channel enhancement-type MOSFET. In this figure, the broken line indicates that there is no conducting channel between drain and source, when $V_{GS} = 0$. Due to this fact, this device is also known as "Normally-OFF MOSFET". The drain and source terminals are shown at the

top and bottom end of the broken line. The substrate is internally connected to the source as shown. The arrow points in the direction of channel (or invertion layer), which is created when V_{GS} is increased above $V_{GS(th)}$.



(*a*) N-channel. (*b*) P-channel.

Fig. 18·18. Circuit symbols for enhancement-type MOSFET.

Fig. 18·18 (*b*) shows the circuit symbol for the P-channel enhancement-type MOSFET. This symbol is similar to N-channel except that the arrow points outwards. This indicates that the channel (or invertion layer) created in the substrate is of P-type. In actual practice, the N-channel and P-channel enhancement-type MOSFET's are known as NMOS and PMOS field-effect transistors respectively.

Example 18·3. *The data sheet for a certain enhancement-type MOSFET reveals that* $I_{D(on)} = 10$ *mA at* $V_{GS} = -12$ *V and* $V_{GS(th)} = -3$ *V. Is this device P-channel or N-channel ? Find the value of* I_D, *when* $V_{GS} = -6$ *V.* (*Oxford University*)

Solution. Given : $I_{D(on)} = 10$ mA ; $V_{GS} = -12$ volts and $V_{GS(th)} = -3$ volts.

Since the value of V_{GS} is negative for the enhancement-type MOSFET, this indicates that the device is P-channel. We know that the drain current,

$$I_D = K\,[V_{GS} - V_{GS(th)}]^2 \qquad \ldots(i$$

or
$$I_{D(on)} = K\,[(V_{GS} - V_{GS(th)}]^2$$
$$10 = K\,[-12-(-3)]^2 = 81\,K$$
$$\therefore \quad K = 10/81 = 0{\cdot}12 \text{ mA/V}$$

Substituting this value of K and V_{GS} (equal to -6) in the equation (*i*),

$$I_D = 0{\cdot}12\,[-6-(-3)]^2 = 1{\cdot}08 \text{ mA}$$ **Ans.**

18·22. The MOSFET as a Resistor

The MOSFETs have an important property that they can be used as a resistor, capacitor, amplifier and a switch. This makes the design of electronic circuits very simple, because the entire circuit consists of only MOSFETs and no other component. The examples of such circuits are microprocessors and memory circuits.

lar than transistor amplifier. The field-effect transistor amplifier is suitable as an input amplifier for low-level signal. Thus it is extensively used in h_i-f_i frequency modulated (FM) receivers.

In this chapter. We shall first discuss the biasing of field-effect transistors (*i.e.* FET's) and then the FET amplifiers.

31·2. Biasing the FET

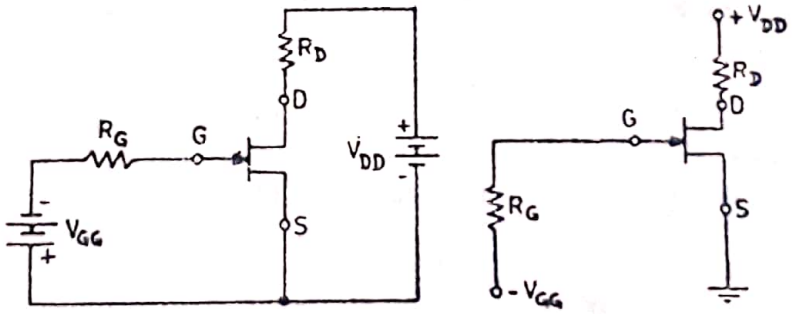
The purpose of biasing a transistor is to select the proper operating point and maintain it, even if there are variations in temperature or among individual devices of the same type. It is done by selecting the suitable values of gate-to-source voltage (V_{GS}) and drain current (I_D). It will be interesting to know that the FET's are used mainly as small-signal amplifiers. It is because of the fact that the transfer characteristic of FET's *i.e.* parabolic in shape and it introduces amplitude distortion, if the signals are large. Therefore if the excursions along the load line are small, the biasing requirements are not critical. In order to make the study more convenient, we shall discuss separately the biasing concept of the junction field-effect transistors (JFET's) and metal-oxide semicondutor field-effect transistor (MOSFET's).

32·3. Biasing the JFET

Although the JFET can be biased in a number of ways, like bipolar transistor, yet the following ways are important from the subject point of view :

1. Gate bias. 2. Self bias. 3. Voltage divider bias. 4. Source bias. 5. Current source bias.

32·4. Gate Bias



(*a*) (*b*)

Fig. 32·1. Gate bias for N-channel JFET.

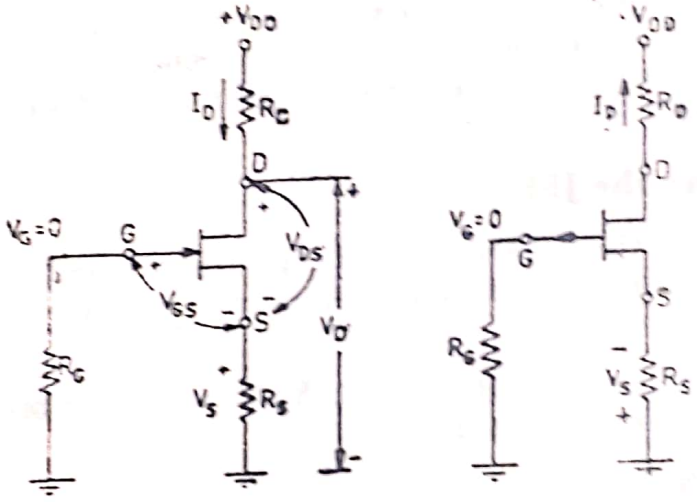
Fig. 32·1 (*a*) shows the gate bias circuit for the N-channel JFET. A more simpler way to draw this circuit is as shown in Fig. 32·1(*b*). We know that the JFET is operated in such a way that gate-source junction is always reverse biased. This condition requires a negative gate-to-source voltage (V_{GS}) for N-channel JFET and positive gate-to- source voltage for P-channel JFET.

The gate bais is the worst possible method to set up the d.c. operating currents and voltages for the JFET, because it gives a

large variation in its drain current. It is due to this reason that the gate-bias method is rarely used in actual practice.

32·5. Self Bias

Fig. 32·2 (*a*) shows the self bias circuit for an N-channel junction field-effect transistor (JFET. In this circuit, there is only one drain supply and no gate supply. The gate terminal is connected through a resistor (R_G) to the ground. The source terminal is connected through a resistor (R_S) to the ground. When the drain voltage is applied, a drain current flows even if there is no gate voltage (V_G). The drain current produces a voltage drop across resistor R_S (equal to $I_D.R_S$). This voltage drop produces the gate-to-source reverse voltage required for an FET operation. The resistor R_S is called a feedback resistor. Its function is to prevent any variation in the FET drain current, which may be understood from the following discussion.



(*a*) For N-channel JFET. (*b*) For P-channel JFET.

Fig. 32·2. Self bias.

First of all, consider an increase in drain current, which will increase the voltage drop across the resistor (R_S). The increased voltage drop increases the reverse gate-to-source voltage, which decreases the effective width of the channel. It reduces the value of drain current. Now, if the drain current decreases, then the reverse action takes place, *i.e.* the reduced drain current decreases the gate-to-source voltage, which inturn increases the effective width of channel, thereby increasing the of value of drain current.

Fig. 32·2 (*b*) shows the self-bias circuit for P-channel JFET. It is similar to N-channel JFET circuit, except that the polarity of drain supply voltage (*i.e.* V_{DD}) is reversed. We know that in a JFET, no current flows through the gate terminal to the ground becaused the gate-source junction is reverse biased. In actual practice, a small current called reverse leakage current (I_{GSS}) does flow through the gate terminal. Usually, its value is very small and can be neglected. Therefore we shall assume that the gate terminal is at zero voltage. In other words, the gate voltage with respect to

ground, *i.e.* $V_G = 0$. We know that the source voltage with respect to ground,

$$V_S = I_D.R_S$$

and the drain voltage,

$$V_D = V_{DD} - I_D.R_D$$

The drain-to-source voltage (V_{DS}) is equal to the difference between the drain voltage (V_D) and the source voltage (V_S).

i.e.,
$$V_{DS} = V_D - V_S = (V_{DD} - I_D.R_D) - I_D.R_S$$
$$= V_{DD} - I_D(R_D + R_S)$$

The gate-to-source voltage (V_{GS}) is equal to the difference between the gate voltage (V_G) and the source voltage (V_S).

i.e.,
$$V_{GS} = V_G - V_S$$
$$= 0 - I_D.R_S$$
$$= -I_D.R_S \quad ...(i)$$

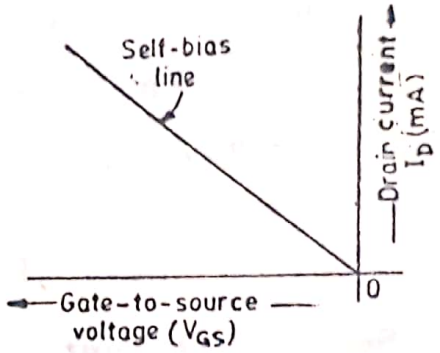


Fig. 32·3. Self bias line.

It is evident from the above relation that the gate-to-source voltage is equal to the negative of the voltage across the source resistor. It is thus obvious that greater the value of drain current, more negative will be the gate-to-source voltage. Rearranging equation (*i*),

$$I_D = -\frac{V_{GS}}{R_S} \quad ...(ii)$$

Now it we plot a graph using the values of drain current obtained from equation (*ii*) for a constrant value of resistor (R_S) against the gate-to-source voltage we get a straight-line as shown in Fig. 32·3. This straight-line is called a self-bias line.

Example 32·1. *Find the values of drain-to-source voltage* (V_{DS}) *and the gate-to-source voltage* (V_{GS}) *for the circuit shown in Fig. 32·4. Given* $I_D = 5\ mA$.

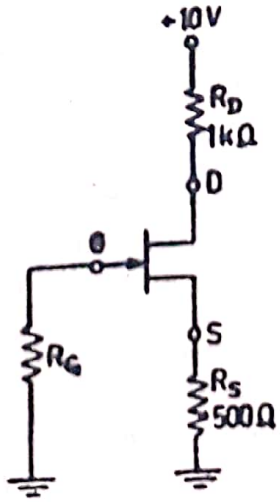


Fig. 32·4

(Calcutta University, 1987)

Solution. Given : $I_D = 5$ mA $= 5 \times 10^{-3}$ A ; $V_{DD} = 10$ volts ; $R_D = 1$ kΩ $= 1 \times 10^3$ Ω and $R_S = 500$ Ω

Drain-to-source voltage

We know that the source voltage,

$$V_S = I_D.R_S = (5 \times 10^{-3}) \times 500 = 2{\cdot}5 \text{ V}$$

and the drain voltage,

$$V_D = V_{DD} - I_D.R_D = 10 - (5 \times 10^{-3}) \times (1 \times 10^3) \text{ V}$$
$$= 10 - 5 = 5 \text{ V}$$

∴ Drain-to-source voltage,

$$V_{DS} = V_D - V_S = 5 - 2{\cdot}5 \text{ V} = 2{\cdot}5 \text{ V}$$ **Ans.**

Gate-to-source voltage,

We know that gate-to-source voltage.

$$V_{GS} = -V_S = -2{\cdot}5 \text{ V}$$ **Ans.**

32·6. Setting a Q-point

We know that the Q-point (quiescent operating point or bias point) for a self-biased JFET is estabilised by determing the value of drain current (I_D) for a desired value of gate-to-source voltage (V_{GS}) or vice versa. However, if the data sheet of a JFET includes a transfer characteristic curve (also called transconductance curve), then we can find the Q-point by using the procedure as given below :

1. First of all, select a convenient value of drain current. Usually, its value is taken half of the maximum possible value of drain current (*i.e.* I_{DSS}). Then find the voltage drop across source resistor (R_S) by the relation,

   $$V_S = I_D.R_S$$

   and the gate-to-source voltage from the relation,

   $$V_{GS} = -V_S$$

2. Now plot the assumed value of drain current (I_D) and the corresponding gate-to-source voltage (V_{GS}) on the transfer characteristic curve.

3. Draw a line through the plotted point and the origin. The point of intesection of the line and the curve gives the desired Q-point. Read the coordinates of Q-point.

As a matter of fact, it is desireable to set the Q-point near the mid-point of the transfer characteristic curve of a JFET. Under signal conditions, the mid-point bias allows a maximum amount of drain current swing between the values of I_{DSS} and O.

Now if we want to design a self-bias current, then any one of the following two methods is used for this purpose :

1. *Analytical method*

In this method, we note down the values of maximum drain current (I_{DSS}) and the gate-to-source cut-off voltage ($V_{GS\,(off)}$) from the data sheets of JFET supplied by the manufacturer. Now the value of drain current is obtained by the relation,

$$I_D = \left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

For example, if we select the gate to source voltage (V_{GS}) equal to $V_{GS(off)}/4$, then the value of drain current,

$$I_D = I_{DSS}[1 - 0{\cdot}25]^2 = I_{DSS}(0{\cdot}75)^2$$

$$= 0{\cdot}56\, I_{DSS}$$

It indicates that the drain current is slighty more than one-half of I_{DSS}. But it will bias the JFET close to the mid-point of the curve. The value of drain resistor (R_D) is selected in such a way that the drain voltage (V_D) is equal to half the drain supply voltage (V_{DD}). The value of gate resistor (R_G) is chosen orbitrarily large, so that it prevents loading on the driving stages.

2. *Graphical method*

In this method, we draw a self-bias line in such a way that it intersects the tranfer characteristic curve near its mid-point. The point of intersection of the self bias line and the transfer characteristic curve gives us the required Q-point. Then read the coordinates of the Q-point. The value of source resistance (R_S) is given by the ratio of gate-to-source voltage (V_{GS}) to the drain current (I_D). Mathematically, the source resistance,

$$R_S = \frac{V_{GS}}{I_D}$$

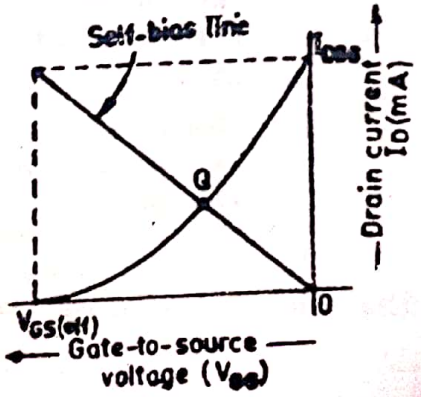


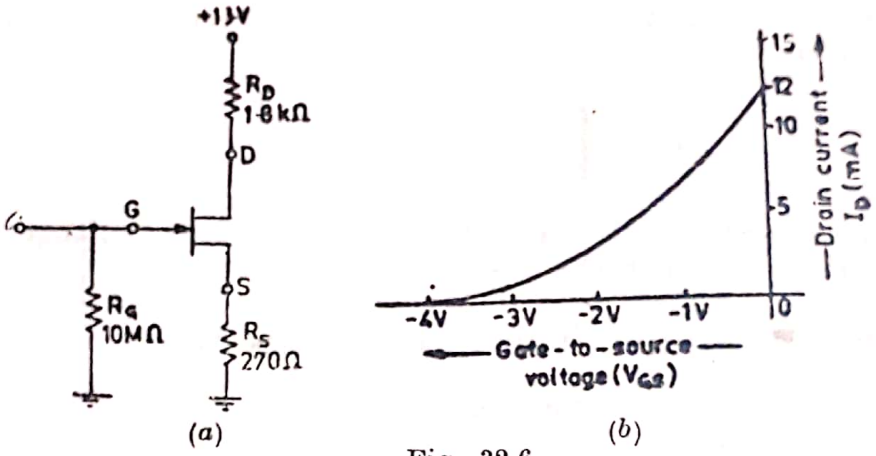
Fig. 32·5. Setting a Q-point.

However, a more accurate method is to draw a self-bias line through the coordinates of I_{DSS} and V_{GS} (off) as shown in Fig. 32·5 Then the point of intersection of self-bias line and the transfer characteristic curve locates the Q-point. The value of source resistor is given by the relation,

$$R_S = \frac{V_{GS(off)}}{I_{DSS}}$$

The value of drain resistor (R_D) and gate resistor (R_G) are selected in the same way as discussed above for the analytical method.

Example 32·2. *Fig. 32·6. (a) shows that circuit of a self-biased JFET amplifier and Fig. 32·6 (b) indicates the transfer characteristic curve of the JFET.*



(a) (b)

Fig. 32·6

Find the quiescent values of I_D and V_{GS}. Calculate the values of d.c. voltage between the drain and ground. (*Birmingham University*)

Solution. Given : $R_D = 1{\cdot}8\ k\Omega = 1{\cdot}8 \times 10^3\ \Omega$; $R_S = 270\ \Omega$; $R_G = 10\ M\Omega$ and I_{DSS} (from transfer characteristic curve) = 12 mA.

(*a*) *Quiescent values of I_D and V_{GS}*

1. First of all, assume the drain current (I_D) equal to the half of I_{DSS} (*i.e.*, 6 mA or 6×10^{-3} A). Using this value of drain current, the voltage drop across resistor (R_S),

$$V_S = I_D.R_S = (6 \times 10^{-3}) \times 270 = 1{\cdot}62\ V$$

and the gate-to-source voltage,

$$V_{GS} = -V_S = -1{\cdot}62\ V$$

2. Now plot the values of drain current (I_D = 6 mA) and the corresponding value of voltage V_{GS} (*i.e.* −1·62 V) on the graph of transfer characteristic curve as shown in Fig. 32·7.

3. Draw a line through the plotted point (P) and the origin as shown in the figure and read the coordinates of Q-point.

It is evident from this graph that the coordinates of Q-point are

$$I_D = 5\ mA$$

$$V_{GS} = -1{\cdot}4\ V\ \textbf{Ans.}$$

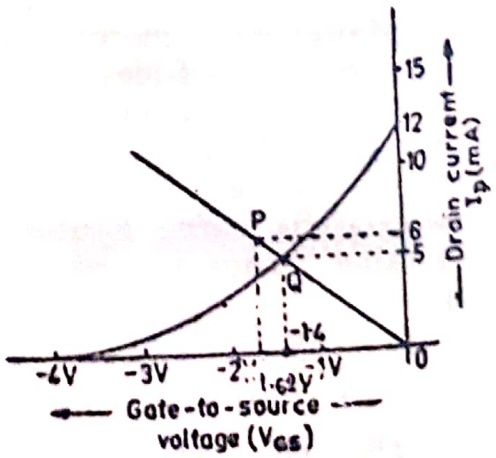


Fig. 32·7

(*b*) *D.C. voltage between drain and ground*

We know that the d.c. voltage between drain and ground,

$$V_D = V_{DD} - I_D.R_D$$
$$= 15 - (5 \times 10^{-3}) \times (1{\cdot}8 \times 10^3)\ V$$
$$= 15 - 9 = 6\ V\ \textbf{Ans.}$$

Example. 32·3. *A self-biased P-channel JFET has a pinch off voltage (V_P) = 5 V and I_{DSS} = 12 mA. The supply voltage available is 12 V. Determine the values of resistors R_D and R_S, so that I_D = 5 mA and V_{DS} = 6 V.* *(Delhi University, 1987)*

Solution. Given : V_P *i.e.* $V_{GS\,(off)}$ = 5 volt ; I_{DSS} = 12 mA $= 12\times10^{-3}$ A ; V_{DD} = 12 volt, I_D = 4 mA $= 4\times10^{-3}$ A and V_{DS} = 6 volt.

We know that the drain current (I_D),

$$4\times10^{-3} = I_{DSS}\left[1-\frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

$$= 12\times10^{-3}\left[1-\frac{V_{GS}}{5}\right]^2$$

$$\frac{1}{3} = \left(1-\frac{V_{GS}}{5}\right)^2$$

$$\frac{1}{\sqrt{3}} = 1-\frac{V_{GS}}{5} \qquad \text{...(Taking square root)}$$

$$\therefore \quad V_{GS} = \left(1-\frac{1}{\sqrt{3}}\right)\times5 = (1-0{\cdot}58)\times5 \text{ V}$$

$$= 2{\cdot}1 \text{ V}$$

We also know that the source voltage,

$$V_S = V_{GS} = 2{\cdot}1 \text{ V}$$

and voltage drop across the source resistor (V_S),

$$2{\cdot}1 = I_D.R_S = (4\times10^{-3})R_S$$

$$\therefore \quad R_S = \frac{2{\cdot}1}{(4\times10^{-3})} = 525\ \Omega \quad \textbf{Ans.}$$

and drain-to source voltage (V_{DS}),

$$6 = V_{DS}-I_D.R_D = 12-(4\times10^{-3})\times R_D$$

$$\therefore \quad = 1500\ \Omega = 1{\cdot}5\ \text{k}\Omega \quad \textbf{Ans.}$$

32·7. Setting a Q-point Using D.C. Load Line

The *Q*-point for the self-biased JFET circuit may also be obtained graphically by using d.c. load line. The d.c. load line may be drawn easily on the drain characteristics as shown in Fig 32·8(*a*) the values of drain current (I_D) and drain-to-source voltage (V_{DS}) at the upper and lower ends of the d.c. load line may be obtained by using the relation,

$$V_{DS} = V_{DD}-I_D(R_D+R_S) \qquad \text{...(i)}$$

At the upper end (*i.e.*, point *A*), the value of drain-to-source voltage (V_{DS}) is equal to zero. Therefore substituting $V_{DS} = 0$ in equation (*i*),

$$0 = V_{DD}-I_D.(R_D+R_S)$$

$$\therefore \qquad I_D = \frac{V_{DD}}{(R_D + R_S)}$$

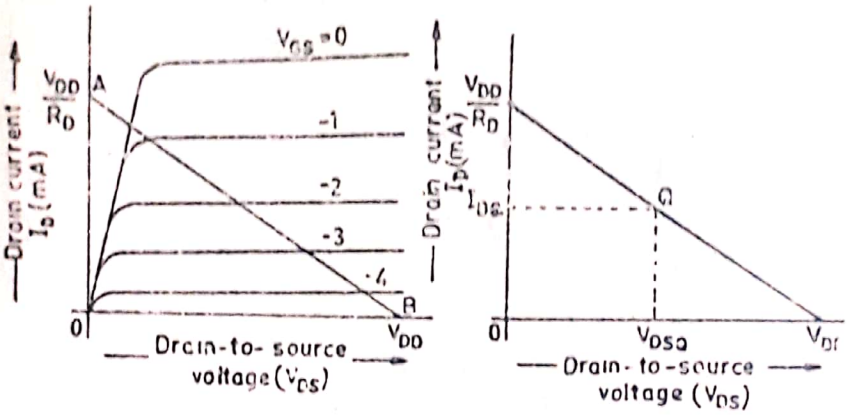
Similarly, at the lower end (*i.e.*, point *B*) the value of drain current (I_D) is equal to zero. Therefore substituting, $I_D = 0$ in equation (*i*),

$$V_{DS} = V_{DD} - 0(R_D + R_S) = V_{DD}$$

Thus the upper and lower ends of the d.c. load line are given by the points,

$$I_D = V_{DD}/(R_D + R_S) \quad \text{and} \quad V_{DS} = 0 \qquad \text{...(Upper end}$$

$$I_D = 0 \text{ and } V_{DS} = V_{DD} \qquad \text{...(Lower end)}$$



(*a*) Drawing d.c. load line. (*b*) Setting a *Q*-point.

Fig. 32·8

The *Q*-point is set at the mid-point of the d.c. load line as shown in Fig. 34·8(*b*). In that case, the value of drain current at *Q*-point,

$$I_{DQ} = \frac{V_{DD}}{2(R_D + R_S)}$$

and the drain-to-source voltage at the *Q*-point,

$$V_{DSQ} = \frac{V_{DD}}{2}$$

Example. 32·4. *Calculate the* ***self-bias*** *operation point for the* ***FET*** *circuit shown in Fig. 32·9.*

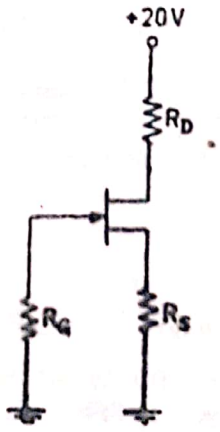


Fig. 32·9

Also calculate the values of resistors R_D and R_S to obtain this bias condition. Given the maximum value of drain current as 10 mA and $V_{GS} = -2{\cdot}2$ V at $I_D = 5$ mA. (*Andhra Universitly, 1987*)

Solution. Given : $I_{DSS} = 10$ mA and $V_{DD} = 20$ volt.

(*a*) *Operating point*

We know that the value of drain current at *Q*-point,

$$I_{DQ} = \frac{I_{DSS}}{2} = \frac{10}{2} = 5 \text{ mA}$$

and the value of drain-to-source voltage,

$$V_{DSQ} = \frac{V_{DD}}{2} = \frac{20}{2} = 10 \text{ V}$$

$\therefore$ Operating point,

$$I_D = 5 \text{ mA} \quad \text{and} \quad V_{DS} = 10 \text{ V} \quad \textbf{Ans.}$$

(*b*) *Values of R_D and R_S*

Here $V_{GS} = -2{\cdot}2$ volt and $I_D = 5 \text{ mA} = 5 \times 10^{-3}$ A

We know that the drain-to-source voltage (V_{DS}),

$$10 = V_{DD} - I_D.R_D = 20 - (5 \times 10^{-3})\, R_D$$

$$\therefore \qquad R_D = \frac{20-10}{5 \times 10^{-3}} = 2 \times 10^3 \ \Omega = 2 \text{ k}\Omega \quad \textbf{Ans.}$$

We also know that the source voltage,

$$V_S = -V_{GS} = -(-2{\cdot}2) = 2{\cdot}2 \text{ V}$$

and the value of voltage drop across the source resistor (V_S),

$$2{\cdot}2 = I_D.R_S = (5 \times 10^{-3}) \times R_S$$

$$\therefore \qquad R_S = 2{\cdot}2/(5 \times 10^{-3}) = 440 \ \Omega \quad \textbf{Ans.}$$

32·8. Biasing Against Device Parameter Variation

We have already discussed that for a self-biased JFET, the *Q*-point is set at the mid point of the transfer characterististic curve. However, it has been found that the JFET parameters like maximum drain current (I_{DSS}) and the gate-to-source cut-off ($V_{GS\,(off)}$) vary with the temperature. In that case, the *Q*-point will also vary with the temperature and hence will not remain stable. This degrades the performance of the FET amplifier circuit.

In order to provide compensation for the device parameter variation, the manufacturers provide two transfer characteristic

curves as shown in Fig. 32·10. The first curve corresponds to the maximum values of I_{DSS} and $V_{GS\,(off)}$. In such a case, we draw a bias line through both the curves, which is near the mid-point of either curve. Then read the values of gate-to-source voltage (V_{GS}) and the drain current (I_D) for either Q-point. The optimum value of source resistor (R_S) is given by the ratio of gate-to-source voltage (V_{GS}) and drain current (I_D).

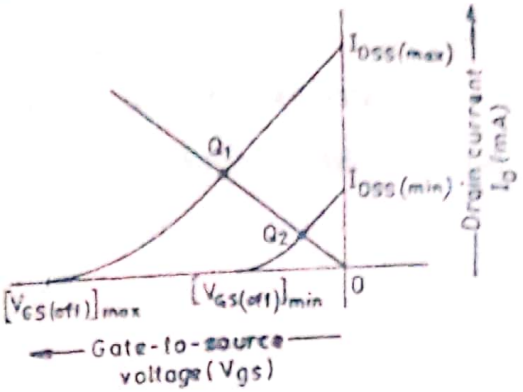


Fig. 32·10. Use of two transfer characteristic curves for setting a Q-point.

Sometimes, the manufacturers do not supply the transfer characteristic curves, but provide the maximum and minimum values of the I_{DSS} and $V_{GS(off)}$. In that case, we calculate the maximum and minimum values of source resistor (R_S) and then take the average of these two values. This average value will provide a Q-point near the mid-point of the either transfer characteristic curve.

32·9. Voltage Divider Bias

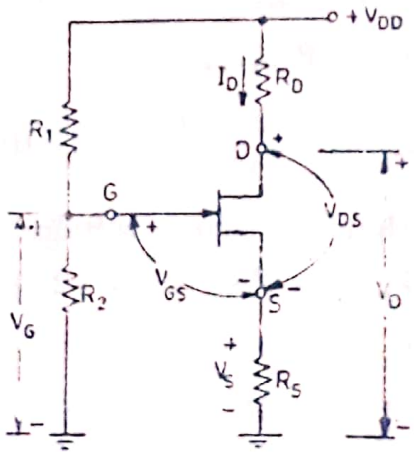


Fig. 32·11. Voltage divider bias.

Fig. 32·11 shows the voltage divider bias circuit. The name 'voltage divider' is derived from the fact that resistors R_1 and R_2 are connected on the gate side (between the V_{DD} supply and ground) form a voltage divider. Assuming the current to be zero, the voltage is given by the relation,

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD}$$

and the voltage from source to ground,

$$V_S = V_G - V_{GS}$$

$\therefore$ Value of drain current,

$$I_D = \frac{V_S}{R_S} = \frac{V_G - V_{GS}}{R_S} \qquad \ldots(i)$$

and the d.c. voltage from drain to ground,

$$V_D = V_{DD} - I_D.R_D$$

Now, if the gate voltage is very large, as compared to gate-to-source voltage, then the drain current is approximately constant for any JFET. It has been found that in actual practice the voltage divider bias is less effective with JFET's than bipolar transistors. It is because of the fact that in bipolar transistors the base-to-emitter voltage (V_{BE}) is approximately 0·7 V with only minor variations from one transistor to next. However, in a JFET, the gate-to-source voltage (V_{GS}) can vary several volts from one JFET to another. As a result of this, it is difficult to make gate voltage (V_G) large enough than the gate-to-source voltage (V_{GS}).

32·10. Source Bias

Fig. 32·12 shows the circuit of a source bias for JFET. It may be noted that this circuit is similar to the emitter bias circuit used for biasing bipolar transistors.

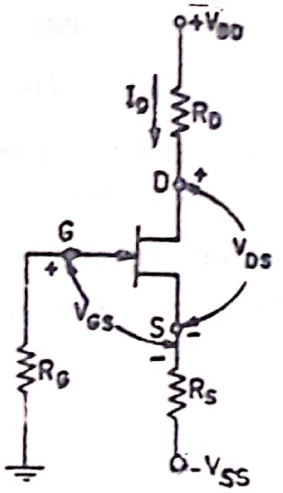


Fig. 32·12. Source bias.

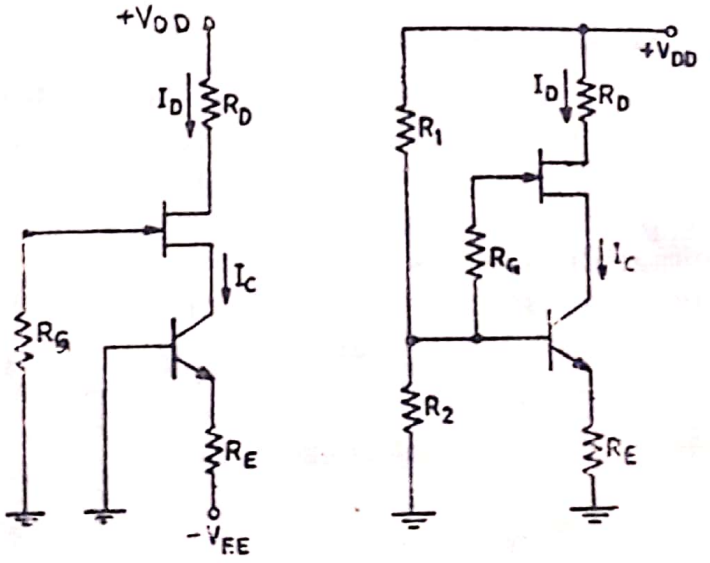
The value of drain current is given by the relation,

$$I_D = \frac{V_{SS} - V_{GS}}{R_S}$$

Since $V_{SS} >> V_{GS}$, therefore drain current,

$$I_D \approx \frac{V_{SS}}{R_S}$$

32·11. Current Source Bias



(*a*) Two supply circuits. (*b*) One supply circuit.

Fig. 32·13. Current-source bias circuit.

Fig· 32·13 shows the current-source bias circuit for a JFET. The circuit of Fig. 32·13 (*a*) uses two supplies (positive and negative), while that of Fig. 32·13 (*b*) employs only one (*i.e.*, positive) supply.

First of all, consider the two supply current-source bias circuit. Here the bipolar transistor is emitter biased. Therefore its collector current is given by the relation,

$$I_C = \frac{V_{EE} - V_{BE}}{R_E} = \frac{V_{EE}}{R_E} \quad \text{...(If } V_{EE} >> V_{BE}\text{)}$$

The drain current of the JFET is equal to the collector current because the bipolar transistor acts like a d.c. current-source, *i.e.*,

$$I_D = I_C$$

Now consider the one supply current-source bias circuit. Here the bipolar transistor is voltage divider biased. Its collector current is given by the relation,

$$I_C = \frac{V_B - V_{BE}}{R_E}$$

and the drain current,

$$I_D = I_C$$

The current-source bias circuit provides a solid Q-point with JFET. Hence this circuit is very useful in actual practice.

32·12. Biasing the Enhancement Type MOSFET's

We have already discussed in the chapter on field-effect transistors that the operation of an enchancement type MOSFET requires a gate-to-source voltage greater than its threshold value (*i.e.*, $V_{GS} > V_{GS(th)}$). This eliminates the use of self-bias because it makes the gate voltage negative with respect to source. There are two methods for biasing the enhancement type MOSFET's namely the voltage divider bias and the drain feedback bias. The voltage divider bias has been already discussed in Art 32·9. The drain feedback bias is similar to the collector feedback bias of bipolar transistors and is discussed as below :

Fig. 32·14 shows the circuit of a drain feedback bias. It may be noted that this type of bias is used only for enhancement type MOSFET's. Since the value of gate current in FET's is approximately zero, therefore there is no voltage drop across gate resistor (R_G). This makes the gate-to-source voltage equal to the drain-to-source voltage, *i.e.*,

$$V_{GS} = V_{DS}$$

The value of drain current is given by relation,

$$I_D = \frac{V_{DD} - V_{DS}}{R_D}$$

The drain feedback bias provides a stable Q-point, because it tends to compensate for any changes in device parameter variation.

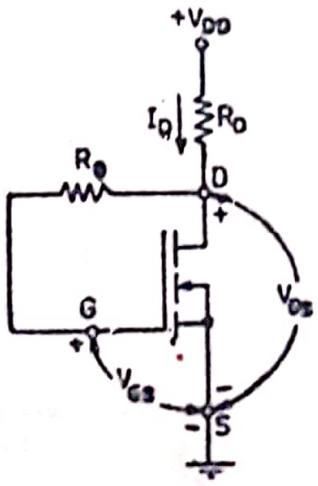
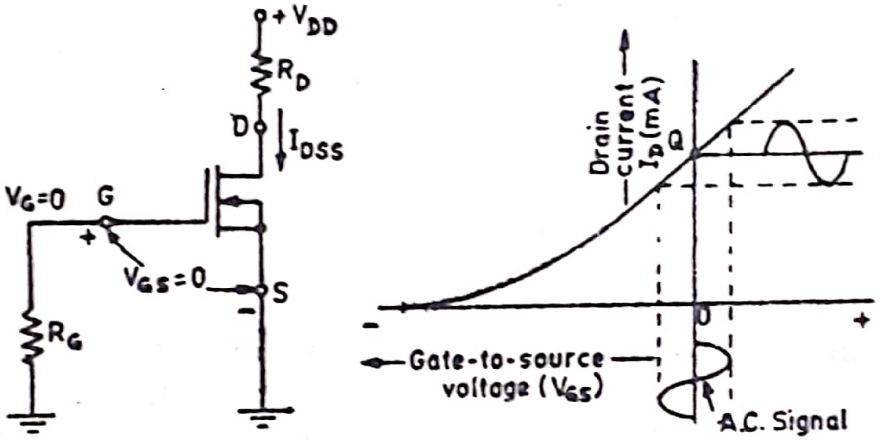


Fig. 32·14. Drain feedback bias.

32·13. Biasing the Depletion Type MOSFET's

We have already discussed in the chapter on field-effect transistors that the depletion type MOSFET can be operated with either positive or negative values of gate-to-source voltage (V_{GS}). Therefore the simplest method is to set the gate-to-source voltage equal to zero as shown in Fig. 32·15 (*a*). This will bias the MOSFET at a point lying on the vertical axis of the transfer characteristic curve as shown in Fig. 32·15 (*b*). If an a.c. signal is applied at the gate, it will vary the gate-to-source voltage above and below the *Q*-point.



(*a*) Bias circuit for depletion type MOSFET.

(*b*) Location of *Q*-point on the transfer characteristic curve.

Fig. 32·15

It may be noted that the biasing circuit of a depletion type MOSFET has no applied gate or source voltage. Therefore the gate-to-source voltage is equal to zero and the drain current is equal to its maximum value (*i.e.*, $I_D = I_{DSS}$). The drain-to-source voltage is given by the relation,

$$V_{DS} = V_{DD} - I_D.R_D = V_{DD} - I_{DSS}.R_D$$

It may be noted that the zero bias is possible only with depletion type MOSFET. It cannot be used for biasing the JFET or bipolar transistor. However, all the biasing methods, discussed for the JFET, can be used for depletion type MOSFET in the depletion mode but not in enhancement mode.

32·14. Small-Signal FET Models

The small-signal FET *model (valid both for JFET and MOSFET) is used to relate small changes in FET current and voltages about the quiescent operating point. The model is different at low-and high-frequencies. Therefore we shall study the small-signal models separately as the low-frequency FET model and high-frequency model. In both these models, the FET will be considered in common source configuration.

32·15. Small-Signal Low-Frequency FET Model

Fig. 32·16 shows the small-signal low-frequency model of a field-effect transistor. In this model, the gate-to-source junction is represented by an open circuit and no current is drawn by the input terminal of the field-effect transistor. It is because of the fact, that the input resistance (i.e., the resistance of gate-source junction) is very large. Its value at d.c. or zero frequency is typically 10^8 to 10^{10} Ω for JFET's and 10^{10} to 10^{14} Ω for MOSFET's. For all practical purposes, these values can be considered to be so large that the input of FET can be considered as an open circuit.

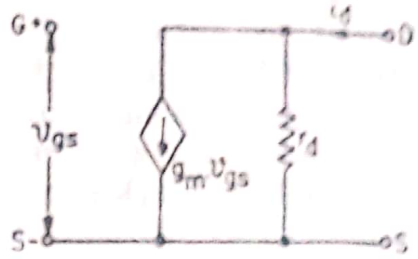
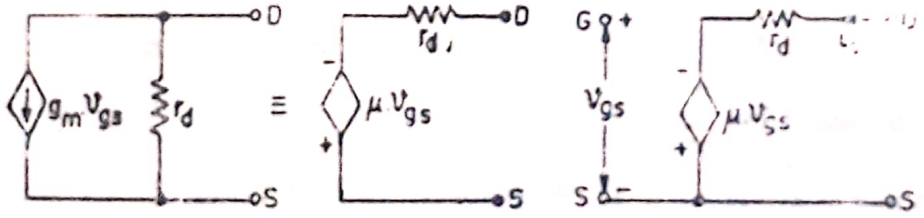


Fig. 32·16. Low-frequency FET model.

It will be interesting to know that although the gate-source junction appears as an open circuit, yet the gate-to source voltage affects the value of drain current. It is indicated by a voltage-controlled current source ($g_m.v_{gs}$) whose value is proportional to the gate-to-source voltage. The FET transconductance (g_m) is measured in milliamperes per volt (mA/V), milli siemens (mS) or milli mhos (m℧). Typical values of transconductance are from 0·5 mA/V to 10 mA/V for JFET's and 0·5 mA/V to 20 mA/V for MOSFET's.

The FET drain resistance (also called FET output resistance) is represented by the resistance (r_d). Typical values of drain resistance are from 100 kΩ to 1 MΩ for JFET's and 1 kΩ to 50 kΩ for MOSFET's.

It is possible to convert the voltage-controlled current source ($g_m.v_{gs}$) into its equivalent voltage-controlled voltage source as shown in Fig. 32·17 (a).



(a) Voltage-controlled current source with its equivalent voltage-controlled voltage source.

(b) Another form of low-frequency FET model.

Fig. 32·17.

The equivalent circuit consists of a voltage-controlled voltage source ($\mu.v_{gs}$) in series with the drain resistance (r_d). The parameter (μ) is the amplification factor of the field effect transistor and its value is equal to the product of transconductance (g_m) and the drain resistance (r_d). Mathematically, the amplification factor,

$$\mu = g_m.r_d$$

Fig. 32·17 (b) shows another form of the low frequency model of a field effect transistor using the voltage source representation.

Sometimes this representation is also very useful in analysing the FET amplifiers.

32·16. Small-Signal High-Frequency FET Model

Fig. 32·18 shows the small-signal high-frequency model of a field-effect transistor. It is identical to the low-frequency model, except the addition of capacitances between each pair of terminals. The capacitor, (c_{gs}) represents the barrier capacitance between the gate and source. Its typical value is from 1 pF to 10 pF for both JFET's and MOSFET's The capacitor (C_{gd}) represents the barrier capacitance between the gate and drain. Its typical value is also from 1 pF to 10 pF for both JFETs and MOSFETs. Similarly, the capacitor (C_{ds}) represents the drain-to-source capacitance. The typical value of C_{ds} is from 0·1 pF to 1 pF.

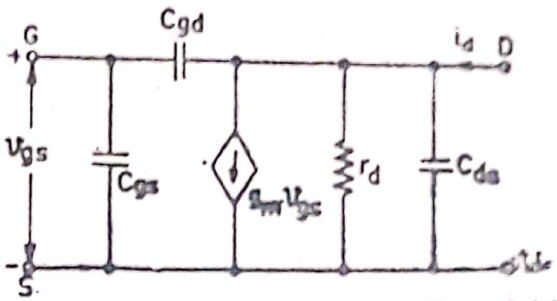


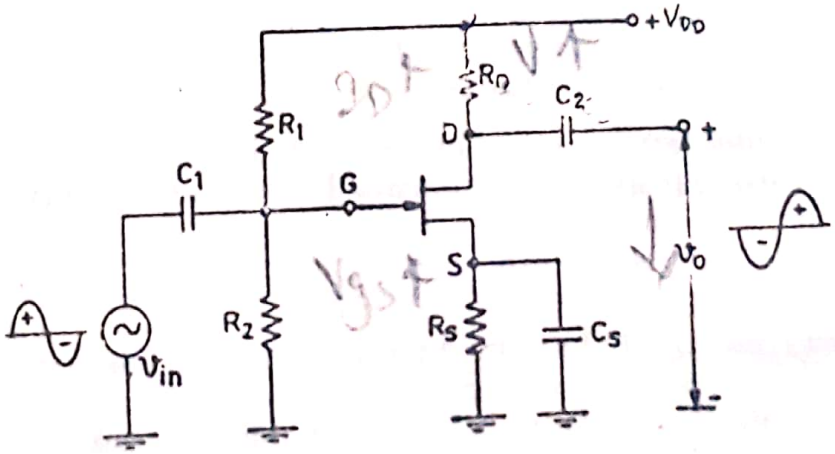
Fig. 32·18. High-frequency FET model

32·17. Field-Effect Transistor Amplifier

The field-effected transistor (FET) has a capability to amplify a.c. signals like a bipolar transistor. Depending open the configuration, the FET amplifiers may be studied under the following three heads :

1. Common source amplifier,
2. Common drain amplifier, and
3. Common gate amplifier.

32·18. Common Source Amplifier



F(g. 32·19. Common source amplifier.

Fig. 32·19 shows the circuit of a common source N-channel JFET amplifier. It is similar to a common emitter amplifier. Here the resistors R_1 and R_2 (called a voltage divider) are used to bias the field-effected transistor. The capacitors (C_1) and (C_2) are used to couple the a.c. input voltage source and the output voltage respectively, these are known as coupling capacitors. The capacitor

(C_S) keeps the source of the FET effectively at a.c. ground and is known as bypass capacitor.

The operation of the circuit may be understood from the assumption that when a small a.c. signal is applied to the gate, it produces variations in the gate-to-source voltages. This produces variations in the drain current. As the gate-to-source voltage increases, the drain current also increases. As a result of this, the voltage drop across the resistor (R_D) also increases. This causes the drain voltage to decrease. It means that the positive half cycle of the input voltage produces the negative half cycle of the output voltage. In other words, the output voltage (at the drain) is 180° out-of-phase with the input voltage (at the gate). This phenome-non of phase inversion is similar to that exhibited by a common emitter bypolar transistor amplifier.

32·19. Analysis of Common Source Amplifier

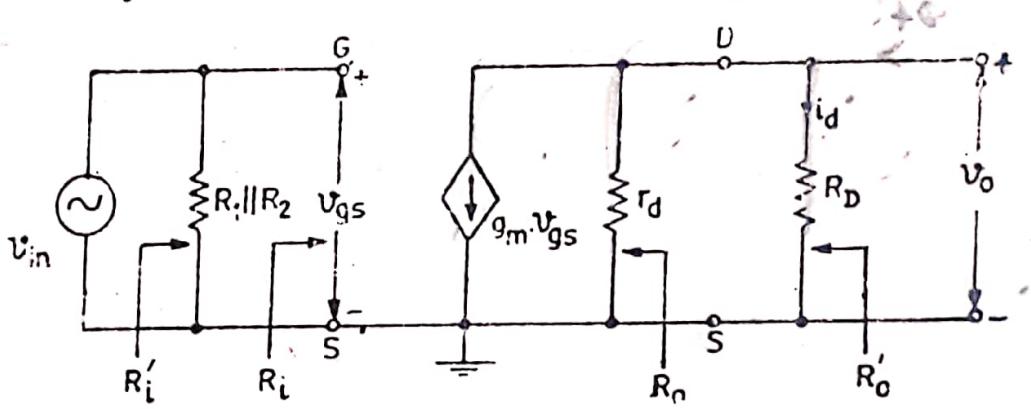


Fig. 32·20. A.C. equivalent circuit of a common source amplifier.

Fig. 32·20 shows the a.c. equivalent circuit of a common source amplifier. This circuit has been obtained from the amplifier circuit shown in Fig. 32·19 by short-circuiting the capacitors and the d.c. voltage supplies. The field-effect transistor is also replaced by its low-frequency model (or equivalent circuit). Now we shall use this circuit to find the expressions for amplifier voltage gain, *input resistance and output resistance.

1. *Voltage gain.* It is the ratio of the output voltage (v_o) to the input voltage (v_{in}). Mathematically the voltage gain,

$$A_v = \frac{v_o}{v_{in}}$$

It may be noted that the current from the current source splits between the resistors r_d and R_D. The current through resistor R_D (as per current divider rule) is given by the relation,

$$i_d = \frac{r_d}{R_D + r_d} (g_m.v_{gs})$$

and the output voltage,

$$v_o = -i_d.R_D = -\left(\frac{r_d}{R_D + r_d}\right)(g_m.v_{gs})R_D$$

$$= -g_m\left(\frac{r_d.R_D}{R_D + r_d}\right)v_{gs}$$

$$= -g_m(r_d \parallel R_D).v_{gs}$$

$$= -g_m.r_L.v_{gs} \qquad \ldots(\because r_L = r_d \parallel R_D)$$

$$= -g_m.r_L.v_{in} \qquad \ldots(\because v_{in} = v_{gs})$$

The minus sign indicates that the output voltage is 180° out-of-phase with the input voltage.

∴ Voltage gain,

$$A_v = \frac{v_o}{v_{in}} = -g_m.r_L$$

It may be noted that if the drain resistance (r_d) is sufficiently greater than resistor R_D, (*i.e.*, $r_d \geqslant 10\ R_D$) then the equivalent resistance of the resistors r_d and R_D in parallel,

$$r_L = R_D$$

and the voltage gain,

$$A_v = g_m.R_D$$

Note ; If the resistance R_D is much larger than r_d (*i.e*, $R_D >> r_d$) then a.c. load resistance (r_L) is approximately equal to r_d. In that case, the amplifier gain is equal to the FFT amplification factor (μ), which is the theoretical maximum voltage gain of the FET. But in actual practice, we can not select R_D to be much larger than r_d because it makes the d.c. bias current in the range of microamperes. The FET transconductance (*i.e.*,g_m) is near zero at this low bias current value.

2. *Input resistance.* It is the ratio of the input voltage (v_{in}) to the input current (i_{in}). Mathematically, the input resistance,

$$R_i = \frac{v_{in}}{i_{in}}$$

We know that input resistance (R_i) of a field-effect transistor is very high and hence can be considered to be infinity (*i.e.*, open-circuit). However, the input resistance of the amplifier stage (R_i') is equal to the parallel combination of resistors R_1 and R_2 and the FET input resistance (R_i). Thus

$$R_i' = (R_1 \parallel R_2) \parallel R_i$$

$$= R_1 \parallel R_2 \qquad \ldots(\text{When } R_i \text{ is infinite})$$

It may be noted that if we use a self-bias circuit (instead of a voltage divider bias), then the input resistance of the amplifier stage,

$$R_i' = R_G$$

3. *Output resistance.* It is the ratio of the output voltage (v_o) to the output current (i_d). Mathematically, the output resistance,

$$R_o' = \frac{v_o}{i_d}$$

We know that the output resistance (R_o) of a field-effect transistor is r_d. But for the amplifier stage, the output resistance is the parallel combination of resistors R_D and r_d *i.e.*,

$$R_o' = R_D \parallel r_d$$

However, if $r_d >> R_D$, then the output resistance of amplifier stage,

$$R_o = R_D$$

Example 32·5. *A certain JFET has a g_m of 4 mS With an external drain resistance of 1·5 kΩ, find the value of ideal voltage gain.*

Solution. Given : $g_m = 4$ mS $= 4 \times 10^{-3}$ S and $R_D = 1{\cdot}5$ kΩ $= 1{\cdot}5 \times 10^3$ Ω.

We know that the voltage gain,

$$A_v = -g_m.R_D = -(4 \times 10^{-3}) \times (1{\cdot}5 \times 10^3)$$
$$= -6 \quad \textbf{Ans.}$$

Example 32.6. *A JFET amplifier has $g_m = 2{\cdot}5$ mA/V and $r_d = 500$ kΩ. The load resistor is 10 kΩ. Find the value of voltage gain.* *(Grad. I.E.T.E., Dec. 1987)*

Solution. Given : $g_m = 2{\cdot}5$ mA/V $= 2{\cdot}5 \times 10^{-3}$ A/V ; $r_d = 500$ kΩ and R_D 10 kΩ.

We know that the a.c. equivalent resistance,

$$r_L = \frac{R_D \times r_d}{R_D + r_d} = \frac{10 \times 500}{10 + 500} \text{ kΩ}$$
$$= 9{\cdot}8 \text{ kΩ} = 9{\cdot}8 \times 10^3 \text{ Ω}$$

∴ Voltage gain,

$$A_v = -g_m.r_L = -(2{\cdot}5 \times 10^{-3}) \times (9{\cdot}8 \times 10^3)$$
$$= -24{\cdot}5 \quad \textbf{Ans.}$$

Example 32·7. *The input and output resistances of the FET amplifier are shown in Fig. 32·21.*

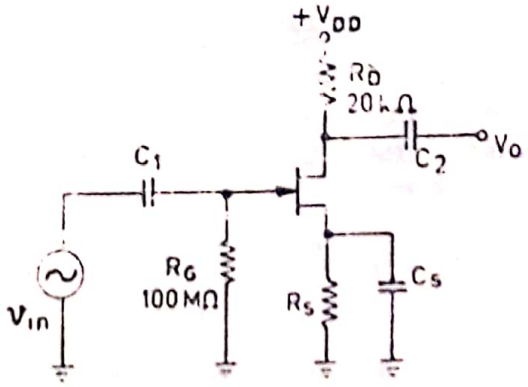


Fig. 32·21.

Calculate the value of voltage gain. The FET amplifier has $g_m = 2$ mA/V and $r_d = 40$ kΩ. *(Birmingham University)*

Solution. Given : $g_m = 2$ mA/V $= 2 \times 10^{-3}$ A/V ; $r_d = 40$ kΩ; $R_D = 20$ kΩ and $R_G = 100$ MΩ.

Voltage gain

We know that the a.c. equivalent resistance,

$$r_L = \frac{R_D \times r_d}{R_D + r_d} = \frac{20 \times 40}{20 + 40} = 13{\cdot}3 \text{ k}\Omega$$

$$= 13{\cdot}3 \times 10^3 \ \Omega$$

∴ Voltage gain,

$$A_v = -g_m . r_L = -(2 \times 10^{-3}) \times (13{\cdot}3 \times 10^3)$$

$$= -26{\cdot}7 \quad \textbf{Ans.}$$

Input resistance

We know that the input resistance,

$$R_i' = R_G = 100 \text{ M}\Omega \quad \textbf{Ans.}$$

Output resistance

We also know that the output resistance,

$$R_o' = r_L = 13{\cdot}3 \text{ k}\Omega \quad \textbf{Ans.}$$

32·20. Effect of A.C. Load on Amplifier Parameters

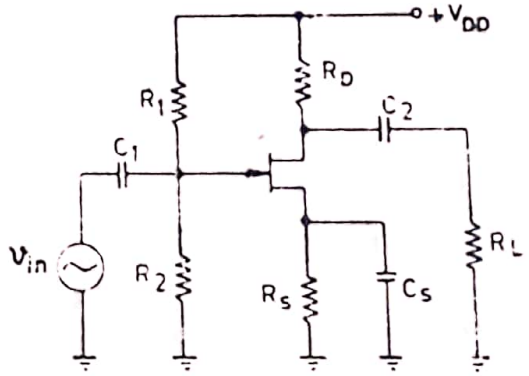


Fig. 32·22. Common source amplifier connected to a load resistor.

Consider a common source amplifier shown in Fig. 32·22. Here a load resistance (R_L) is connected to the amplifier's output through a coupling capacitor. In this case, the total or effective drain resistance is the parallel combination of resistors R_D and R_L *i.e.*,

$$r_L = R_D \parallel R_L$$

It may be noted that in the above expression, if we also consider the FET drain resistance (r_d), then the effective drain resistance,

$$r_L = (R_D \parallel R_L) \parallel r_d$$

The effect of load resistor (R_L) is to reduce the voltage gain as well as the output resistance. The value of voltage gain with load resistance is given by the relation,

$$A_v = -g_m . r_L$$

$$A_u = -g_m (R_D \parallel R_L) \parallel r_d$$
$$= -g_m (R_D \parallel R_L) \quad \text{...(If } r_d >> (R_D \parallel R_L))$$

and the output resistance, of the amplifier stage

$$R_o' = (R_D \parallel R_L) \parallel r_d$$
$$= R_D \parallel R_L \quad \text{...(If } r_d >> (R_D \parallel R_L))$$

Example 32·8. *Fig. 32·23 shows the circuit of a common source FET amplifier.*

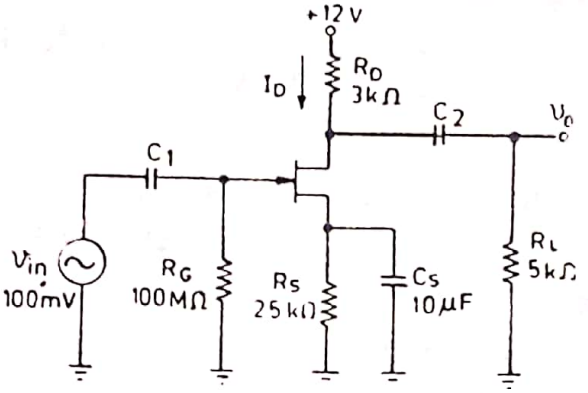


Fig. 32·23.

Find the value of r.m.s. output voltage. The g_m is 4500 μS and I_D is 2 mA. Neglect the FET drain resistance (r_d).

(Jodhpur University, 1988)

Solution. Given : $g_m = 4500\,\mu S = 4500 \times 10^{-6} S$; $R_D = 3$ kΩ $R_L = 5$ kΩ ; $v_{in} = 100$ mV $= 100 \times 10^{-3}$ V and $I_D = 2$ mA.

We know that the effective value of a.c. drain resistance,

$$r_L = R_D \parallel R_L = \frac{R_D \times R_L}{R_D + R_L} = \frac{3 \times 5}{3+5} \text{ kΩ}$$
$$= 1{\cdot}875 \text{ kΩ} = 1875 \text{ Ω}$$

∴ Output voltage,

$$v_o = -g_m . r_L . v_{in}$$
$$= -(4500 \times 10^{-6}) \times (1875) \times (100 \times 10^{-3})$$
$$= 0{\cdot}844 \text{ V} \quad \textbf{Ans.}$$

32·21. Effect of External Source Resistance on Voltage Gain

We have already discussed a field-effect transistor amplifier in which the source resistor is completely bypassed for a.c. signals. It means that for a.c. signals, the source is grounded. Now consider the amplifier circuit in which we include an external resistor (r_S) to the source resistance (R_S) as shown in Fig. 32·24. The source is no longer at a.c. ground. The drain current through resistor (r_S) produces an a.c. voltage between the source and ground.

It may be noted thet the total input voltage between the gate and ground,

$$v_{in} = v_{gs} + i_d.r_s$$

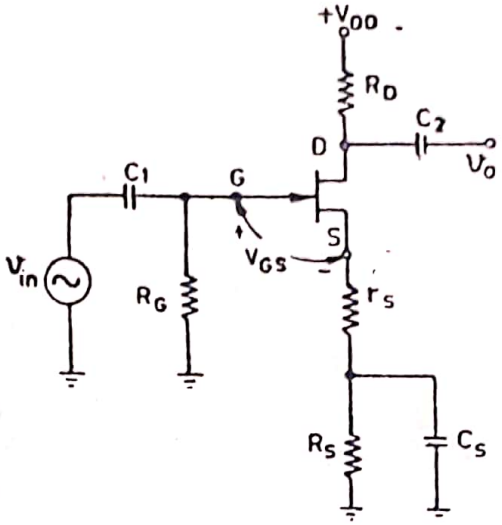


Fig. 32·24. JFET amplifier with external source resistance.

and the output voltage,

$$v_o = - i_d.r_L$$

where r_L is the parallel combination of resistor R_D and the FET ou put resistance (r_d). Therefore voltage gain,

$$A_v = \frac{v_o}{v_{in}} = -\frac{i_d.r_L}{v_{gs} + i_d.r_s}$$

Substituting the value of i_d (equal to $g_m.v_{gs}$) in the abov expression,

$$A_v = -\frac{g_m.v_{gs}.r_L}{v_{gs} + g_m.v_{gs}.r_s} = -\frac{g_m.v_{gs}.r_L}{v_{gs}(1 + g_m.r_s)}$$

$$= -\frac{g_m.r_L}{1 + g_m.r_s} = -\frac{r_L}{r_s + \frac{1}{g_m}}$$

It is evident from the above expression that the external source resitance (r_s) reduces the voltage gain. If the value of resistor r_s is made sufficiently large as compared to $1/g_m$, then the voltage gain,

$$A_v = -\frac{r_L}{r_s}$$

It means that the voltage gain is independent of the changes in the transconductance value. It is known as the swamping effect. Because of this fact the external source resistance (r_s) is referred to as the swamping resistor and the FET amplifier as the swamped amplifier.

Example 32·9. *Fig. 32·25 shows the circuit of a swamped FET amplifier.*

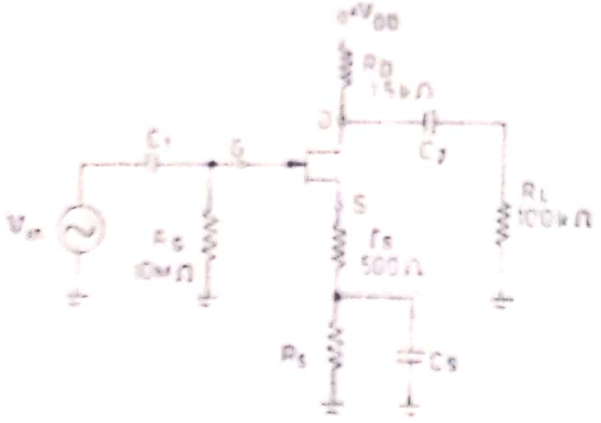


Fig. 32·25

Determine the voltage gain (a) when $R_L = 0$ *and (b) when* R_L *is 100 kΩ. Neglect the FET output resistance* (r_d) *Take* $g_m = 4\ mS$.

(Bhopal Uneversity, 1988)

Solution. Given : $g_m = 4\ mS. = 4 \times 10^{-3}\ S$; $R_D = 1{\cdot}5\ k\Omega$; $R_G = 10\ M\Omega$ and $r_s = 500$.

(a) Voltage gain when R_L *is zero*

We known that the effective a.c. drain resistance,

$$r_L = R_D = 1{\cdot}5 \times 10^3\ \Omega$$

and the voltage gain,

$$A_v = -\frac{g_m . r_L}{1 + g_m . r_s}$$

$$= -\frac{(4 \times 10^{-3}) \times (1{\cdot}5 \times 10^3)}{1 + (4 \times 10^{-3}) \times 500} = -2 \quad \textbf{Ans.}$$

(b) Voltage gain when R_L *is 100 kΩ*

We know that the effective a.c. drain resistance,

$$r_L = \frac{R_D \times R_L}{R_D + R_L} = \frac{1{\cdot}5 \times 100}{1{\cdot}5 + 100} = 1{\cdot}48\ k\Omega$$

$$= 1{\cdot}48 \times 10^3\ \Omega$$

and the voltage gain,

$$A_v = -\frac{g_m . r_L}{1 + g_m . r_s}$$

$$= -\frac{(4 \times 10^{-3}) \times (1{\cdot}48 \times 10^3)}{1 + (4 \times 10^{-3}) \times 500}$$

$$= -1{\cdot}97 \quad \textbf{Ans.}$$

32·22. Common Drain Amplifier

Fig. 32·26 shows the circuit of a common drain amplifier. It is similar to common collector (or emitter follower) amplifier. Self-biasing is used in the circuit. The input signal is applied to the

gate through a coupling capacitor (C_1). And the output is taken from the source terminal through the coupling capacitor (C_2).

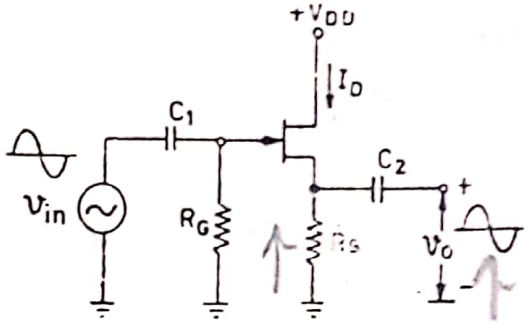


Fig. 32·26. Common drain amplifier.

The operation of the amplifier may be understood by assuming that when a small a.c. signal is applied to the gate, it produces variations in the gate-to-source voltage. This further produces the variations in drain current (I_D). As the gate-to-source voltage increases, the drain current also increases. As a result of this, the voltage drop across the source resistor (R_S) also increases. Thus the output voltage (v_o) increases. It may be noted that the output voltage of a common drain amplifier is approximately equal to and in phase with the input voltage. Because of this fact, the circuit is known as source follower.

A common drain amplifier (or a source follower) has a very high value of input resistance. It is because of this property that a common drain amplifier is used at the front end of measuring instruments like electronic voltmeters and cathode ray oscilloscopes.

32·23. Analysis of a Common Drain Amplifier

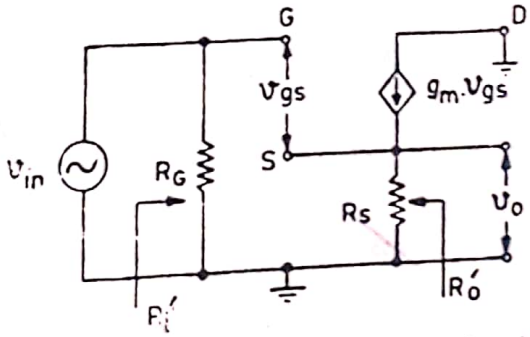


Fig. 32·27. A.C. equivalent circuit of a common drain amplifier.

Fig. 32·27 shows the a.c. equivalent circuit of a common drain amplifier. This circuit has been obtained from the amplifier circuit shown in Fig. 32·26 by short circuiting the capacitors and d.c. voltage supply. The field-effect transistor is also replaced by its low-frequency model. Now we shall use this circuit to find the expressions for voltage gain, input resistance and output resistance.

1. *Voltage gain.* It is the ratio of output voltage (v_o) to the input voltage (v_{in}). Mathmatically, the voltage gain,

$$A_v = \frac{v_o}{v_{in}}$$

For the common drain amplifier, the input voltage,

$$v_{in} = v_{gs} + i_d.R_s$$

and the output voltage,

$$v_o = i_d.Rs$$

$\therefore$ Voltage gain,

$$A_v = \frac{v_o}{v_{in}} = \frac{i_d.R_s}{v_{gs} + i_d.R_s}$$

Substituting the value of $i_d (= g_m.v_{gs})$ in the above expression,

$$A_v = \frac{(g_m.v_{gs})R_s}{v_{gs} + g_m.v_{gs}.R_s}$$

$$= \frac{g_m.v_{gs}.R_s}{v_{gs}(1 + g_m.R_s)}$$

$$= \frac{g_m.R_s}{1 + g_m.R_s} = \frac{R_s}{R_s + \frac{1}{g_m}}$$

It may be noted that when R_s is much greater than $1/g_m$, the value of voltage gain approaches unity.

2. *Input resistance.* We know that the input signal is applied to the gate of the amplifier. As a result of this, the input resistance seen by the input signal source is extremely high just as in the common source configuration. The total input resistance (or the input resistance of the amplifier),

$$R_i' = R_G \parallel R_i$$

where R_i is the input resistance of the field effect transistor. Since the value of R_i is extremely high, therefore the total input resistance,

$$R_i' = R_G$$

3. *Output resistance.* We know that voltage gain of the common drain amplifier,

$$A_v = \frac{v_o}{v_{in}} = \frac{R_s}{R_s + \frac{1}{g_m}}$$

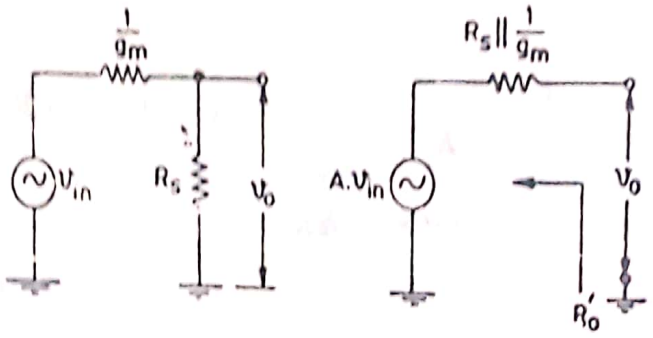
$\therefore$ Output voltage,

$$v_o = \left(\frac{R_s}{R_s + \frac{1}{g_m}} \right) \times v_{in}$$

The above expression is a voltage-divider equation. It implies that the input voltage (v_{in}) drives two resistors R_s and $1/g_m$ with

output voltage taken across resistor (R_s). It means that the output side of the amplifier appears as shown in Fig. 32·28 (*a*). It is evident from this figure, that the source resistor is driven by an a.c. source with an output resistance, *i.e.*,

$$R_D = 1/g_m$$



(*a*) A.C. equivalent circuit of output side of the amplifier (*b*) Thevenin's equivalent circuit of the amplifier.

Fig. 32·28

It may be noted that output resistance (R_o) is the value of resistance looking back into the source terminal of the JFET. Now let us thevenize the output circuit. The resulting circuit is as shown in Fig. 32·28 (*b*). It is evident from this figure, that the resistance R_s is in parallel with $1/g_m$ and the output resistance of the amplifier stage,

$$R_o' = R_s \parallel \frac{1}{g_m}$$

If the value of source resistance (R_s) is much larger than $1/g_m$, then the output resistance of the amplifier stage,

$$R_o' = \frac{1}{g_m}$$

Example 32·10. *Fig. 32·29 shows the circit of a source follower. Determine the voltage gain of the amplifier.*

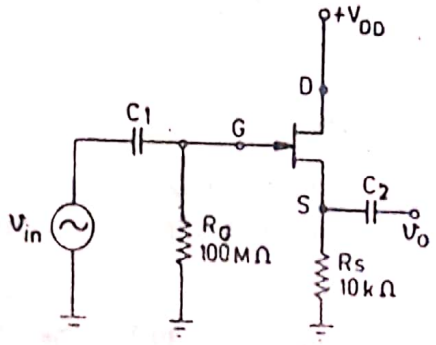


Fig. 32·29

Also determine the input and output resistances of the amplifier. Assume $g_m = 8000\ \mu S$, infinite input resistance and neglect FET output resistance. (Oxford University)

Solution. Given : $g_m = 8000\ \mu S = 8000 \times 10^{-6}\ S$; R_G 10 kΩ $= 10 \times 10^3\ \Omega$ and $R_G = 100\ M\Omega$

47 30 119

Voltage gain

We know that the reciprocal of transconductance,

$$\frac{1}{g_m} = \frac{1}{8000 \times 10^{-6}} = 125\ \Omega$$

and the voltage gain,

$$A_v = \frac{R_s}{R_s + \dfrac{1}{g_m}} = \frac{10 \times 10^3}{(10 \times 10^3) + 125}$$

$$= 0{\cdot}988 \quad \textbf{Ans.}$$

Input resistance

We know that the input resistance

$$R_i' = R_G = 100\ \text{M}\Omega \quad \textbf{Ans.}$$

Output resistance

We also know that the output resistance,

$$R_o' = \frac{1}{g_m} = \frac{1}{8000 \times 10^{-6}} = 125\ \Omega \quad \textbf{Ans.}$$

Example 32·11. *Find the voltage gain for the source follower shown in Fig. 32·30.*

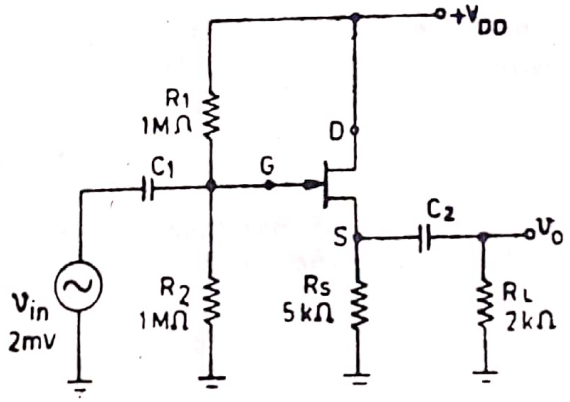


Fig. 32·30

Also find the input and output resistances. If the input voltage is 2 mV, find the value of the output voltage. Assume $g_m = 5500\ \mu S$.

(London Udiversity)

Solution. Given : $v_{in} = 2$ mA ; $g_m = 5500\ \mu S. = 5500 \times 10^{-6}\ S$; $R_1 = R_2 = 1\ \text{M}\Omega$; $R_S = 5\ \text{k}\Omega = 5000\ \Omega$ and $R_L = 2\ \text{k}\Omega = 2000\ \Omega$

Voltage gain

We know that the reciprocal of transconductance,

$$\frac{1}{g_m} = \frac{1}{5500 \times 10^{-6}} = 181{\cdot}8\ \Omega$$

and the voltage gain,

$$A_v = \frac{R_s}{R_s + \frac{1}{g_m}} = \frac{5000}{5000+181\cdot8} = 0\cdot965 \quad \textbf{Ans.}$$

Input resistance

We know that input resistance,

$$R_i' = R_1 \parallel R_2 = \frac{R_1 . R_2}{R_1 + R_2} = \frac{1 \times 1}{1+1} \text{ M}\Omega$$

$$= 0\cdot5 \text{ M}\Omega \quad \textbf{Ans.}$$

Output resistance

We know that the input resistance,

$$R_o' = R_s \parallel \frac{1}{g_m} = 5000 \parallel 181\cdot8$$

$$= 175\cdot4 \ \Omega \quad \textbf{Ans.}$$

Output voltage

Let v_o = Value of the output voltage.

Fig. 32·31. shows the a.c. equivalent circuit of the output side of the source follower. It is evident from this figure, that an a.c. source of voltage $A_v . v_{in}$ (equal to $0\cdot965 \times 2$ or 1·93 V) is in series with an output resistance of 175·4 Ω.

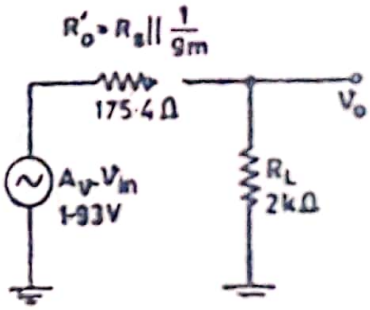


Fig. 32·31

We know that the a.c. voltage across the load resistor,

$$v_o = \left(\frac{R_L}{R_L + R_o'} \right) \times A_v . v_{in}$$

$$= \left(\frac{2000}{2000+175\cdot4} \right) \times 1\cdot93 \text{ mV}$$

$$= 1\cdot77 \text{ mV} \quad \textbf{Ans.}$$

32·24. Common Gate Amplifier

Fig. 32·32 shows the circuit of a common gate amplifier. It is similar to a common base amplifier. The input signal is applied at the source through a coupling capacitor (C_1) and the output is taken from the drain through the coupling capacitor (C_2). The gate is effectively at a.c. ground because of the capacitor, (C_O)

The operation of the common gate amplifier may be under stood from the assumption that when a small a.c. signal is applied to the source, it produces variations in gate-to-source voltage (V_{GS}). This in turn, produces the variations in drain current (I_D). As the gate-to-source voltage increases, the drain current also increases. As a result of this, the output voltage also increases.

Thus output voltage of a common gate amplifier is in phase with the input voltage.

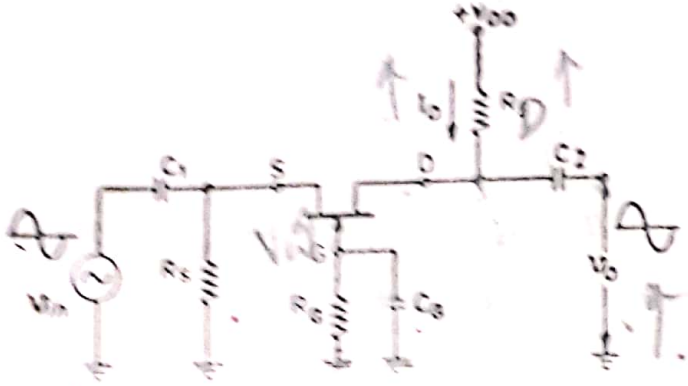


Fig. 32-32. Common gate amplifier.

A common gate amplifier has a low input resistance, high output resistance, high voltage gain and no phase reversal.

32-25 Analysis of a Common Gate Amplifier

Fig. 32-33 shows an a.c. equivalent circuit of a common gate amplifier. This circuit has been obtained from the amplifier circuit shown in Fig. 32-32 by short-circuiting the capacitors and the d.c. supply. The field-effect-transistor is also replaced by its low-frequency model.

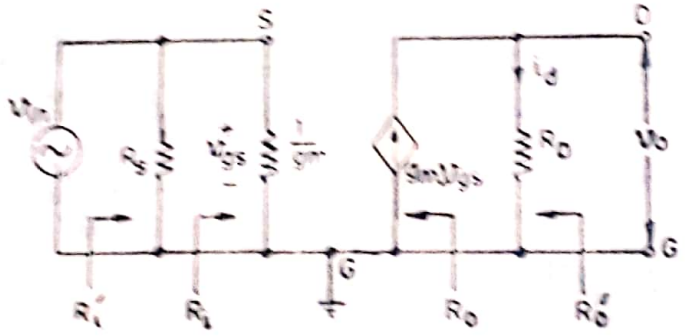


Fig. 32-33. Common gate amplifier.

Now we shall use this circuit to find the expressions for amplifier voltage gain, input resistance and ouput resistance.

1. *Voltage gain.* It is the ratio of a.c. output voltage (v_o) to the a.c. input valtage (v_{in}). Mathematically, the voltage gain,

$$A_v = \frac{v_o}{v_{in}}$$

We know that the a.c. input voltage,

$$v_{in} = v_{gs}$$

and the a.c. output voltage,

$$v_o = i_d . R_D$$

∴ Voltage gain,

$$A_v = \frac{i_d . R_D}{v_{gs}}$$

Substituting the value of i_d (equal to $g_m.v_{gs}$) in the above expression,

$$A_v = \frac{(g_m.v_{gs}).R_D}{v_{gs}} = g_m.R_D$$

It may be noted that the above expression for voltage gain is true only when there is no load resistor. If there is a load resistor (R_L) connected to the amplifier output, then the voltage gain.

$$A_v = g_m(R_D \parallel R_L)$$

2. *Input resistance.* It is the ratio of input voltage (v_{in}) to the input current (i_{in}). Mathematically, the input resistance,

$$R_i = \frac{v_{in}}{i_{in}}$$

For a common gate amplifier, the input voltage (v_{in}) is equal to the gate-to-source voltage (v_{gs}) and the input current (i_{in}) is equal to the drain current (i_d). Therefore the input resistance,

$$R_i = \frac{v_{gs}}{i_d} = \frac{v_{gs}}{g_m.v_{gs}} \quad \ldots(\because \; i_d = g_m.v_{gs})$$

$$= \frac{1}{g_m}$$

It may be noted that the resistance (R_i) is the value of input resistance looking direclty into the source terminal of the JFET. The input resistance of the amplifier,

$$R_i' = R_s \parallel \frac{1}{g_m}$$

However, if R_s is much larger than the reciprocal of transconductance ($1/g_m$), then the input resistance of the amplifier,

$$R_i' = R_s$$

It is evident from the above relation that a common gate amplifier has a low input resistance (equal to the value of external source resistance only). It is in contrast to the common source and common drain amplifier, which have extremely high input resistances.

3. *Output resistance.* It is the ratio of a.c. output voltage (v_o) to the a.c. output current (i_o). Mathematically, the output resistance of the amplifier,

$$R_o' = \frac{v_o}{i_o} = \frac{i_d.R_D}{i_d} \quad \ldots(\because \; v_o = i_d.R_D \text{ and } i_o = i_d)$$

$$= R_D$$

It means that the output resistance of the common gate amplifier is equal to the external drain resistance (R_D). If there is a load resistor (R_L) connected to the amplifier output, then the output resistance of the amplifier,

$$R_o' = R_D \parallel R_L$$

MODULE IV

OPERATIONAL AMPLIFIERS AND LINEAR APPLICATIONS

Georgia Tech

Integrated Circuits

- If multiple electronic components are interconnected on a single chip of semiconductor material, then that chip is called as an Integrated Circuit (IC). It consists of both active and passive components.

Advantages

- **Compact size**: For a given functionality, you can obtain a circuit of smaller size using ICs, compared to that built using a discrete circuit.
- **Lesser weight**: A circuit built with ICs weighs lesser when compared to the weight of a discrete circuit that is used for implementing the same function of IC.
- **Low power consumption**: ICs consume lower power than a traditional circuit, because of their smaller size and construction.
- **Reduced cost**: ICs are available at much reduced cost than discrete circuits because of their fabrication technologies and usage of lesser material than discrete circuits.
- **Increased reliability**: Since they employ lesser connections, ICs offer increased reliability compared to digital circuits.
- **Improved operating speeds**: ICs operate at improved speeds because of their switching speeds and lesser power consumption.

Types

Integrated circuits are of two types:

- Analog Integrated Circuits and
- Digital Integrated Circuits.

Analog Integrated Circuits

- Integrated circuits that operate over an entire range of continuous values of the signal amplitude are called as Analog Integrated Circuits.
- These are further classified into the two types as discussed here:

❖ Linear Integrated Circuits.

❖ Radio Frequency Integrated Circuits.

Linear Integrated Circuits

- An analog IC is said to be Linear, if there exists a linear relation between its voltage and current. IC 741, an 8-pin Dual In-line Package (DIP)op-amp, is an example of Linear IC

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Radio Frequency Integrated Circuits

- An analog IC is said to be Non-Linear, if there exists a non-linear relation between its voltage and current. A Non-Linear IC is also called as Radio Frequency IC.

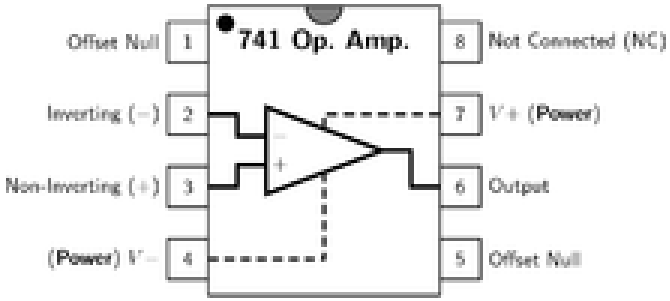
Digital Integrated Circuits

- If the integrated circuits operate only at a few pre-defined levels instead of operating for an entire range of continuous values of the signal amplitude, then those are called as Digital Integrated Circuit

What is an Op-Amp

- An Operational Amplifier (Op-Amp) is an integrated circuit that uses external voltage to amplify the input through a very high gain.
- We recognize an Op-Amp as a mass-produced component found in countless electronics.

What an Op-Amp looks like to a lay-person



What an Op-Amp looks like to an engineer

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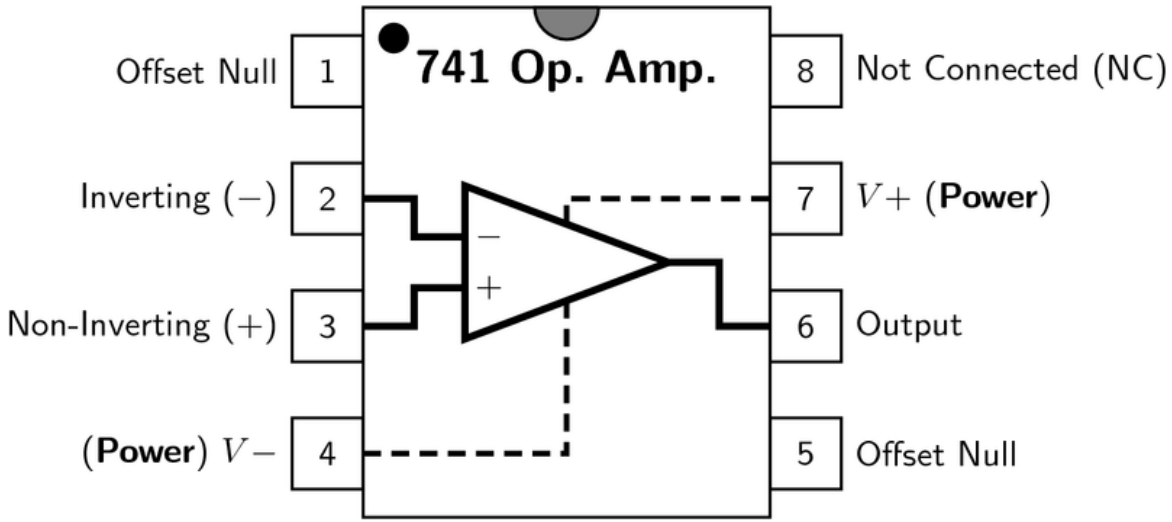
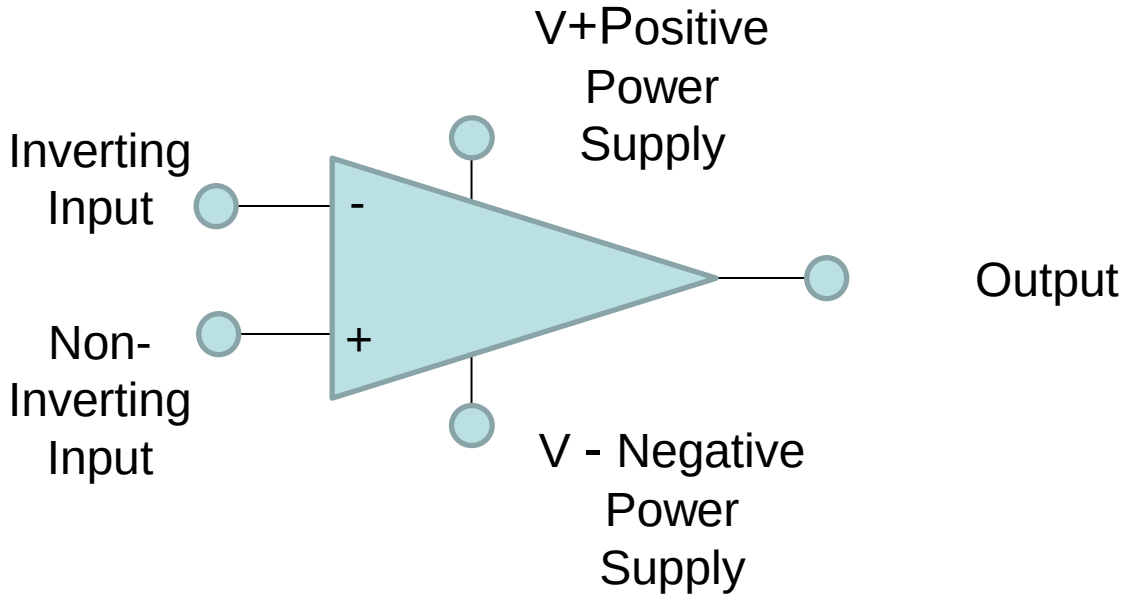
What is an Op-Amp? – The Layout

- There are 8 pins in a common Op-Amp, like the 741 which is used in many instructional courses.



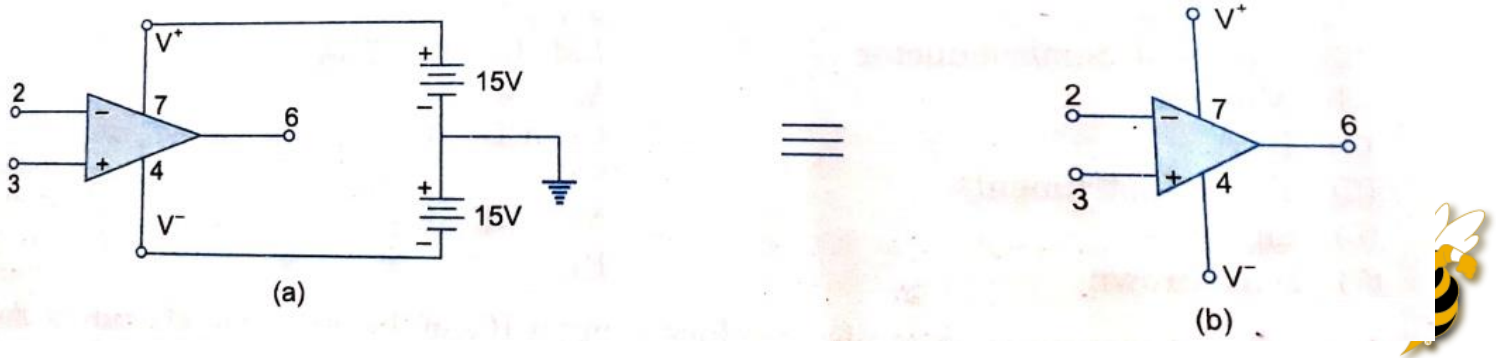
What is an Op-Amp? – The Inside

- The actual count varies, but an Op-Amp contains several Transistors, Resistors, and a few Capacitors and Diodes.
- For simplicity, an Op-Amp is often depicted as this:



Power supply connections

- The V^+ and V^- Power supply terminals are connected to two DC Voltage sources.
- The V^+ pin is connected to the positive terminal of one source and V^- pin is connected to negative terminal of another source .
- The typical values of power supply voltage may range from about $\mp$5V to $\mp$ 22V .
- The common terminal of V^+ and V^- source is connected to reference point or Ground.
- The common point of the two supplies must be grounded, otherwise twice the supply voltage will get applied and it damaged the opamp.



Ideal Characteristics

The schematic symbol of an op-amp is shown in Fig. 2.4 (a). It has two input terminals and one output terminal. Other terminals have not been shown for simplicity. The – and + symbols at the input refer to inverting and non-inverting input terminals respectively, i.e if $v_1 = 0$, output v_0 is 180° out of phase with input signal v_2. And, when $v_2 = 0$, output v_0 will be in phase with the input signal applied at v_1. This op-amp is said to be ideal if it has the following characteristics.

Open loop voltage gain,	A_{OL}	=	∞
Input impedance,	R_i	=	∞
Output impedance	R_o	=	0
Bandwidth	BW	=	∞

Zero offset, i.e. $v_o = 0$ when $v_1 = v_2 = 0$.

Ideal Characteristics

(i) an ideal op-amp draws no current at both the input terminals i.e., $i_1 = i_2 = 0$. Because of infinite input impedance, any signal source can drive it and there is no loading on the preceding driver stage.

(ii) Since gain is ∞, the voltage between the inverting and non-inverting terminals, i.e., differential input voltage $v_d = (v_1 - v_2)$ is essentially zero for finite output voltage v_o.

(iii) The output voltage v_o is independent of the current drawn from the output as $R_o = 0$. The output thus can drive an infinite number of other devices.

The above properties can never be realized in practice. However, the use of such an 'Ideal op-amp' model simplifies the mathematics involved in op-amp circuits. There are practical op-amps that can be made to approximate some of these characteristics.

Ideal Characteristics

A physical amplifier is not an ideal one. So, the equivalent circuit of an op-amp may be shown in Fig. 2.4 (b) where $A_{OL} \neq \infty$, $R_i \neq \infty$ and $R_o \neq 0$. It can be seen that op-amp is a voltage controlled voltage source and $A_{OL}\, v_d$ is an equivalent *Thevenin* voltage source and R_o is the *Thevenin* equivalent resistance looking back into the output terminal of an op-amp. The equivalent circuit is useful in analyzing the basic operating principles of op-amp. For the circuit shown in Fig. 2.4 (b), the output voltage is

$$\begin{aligned} v_o &= A_{OL}\, v_d \\ &= A_{OL}\, (v_1 - v_2) \end{aligned} \qquad (2.1)$$

The equation shows that the op-amp amplifies the difference between the two input voltages.

Ideal Characteristics

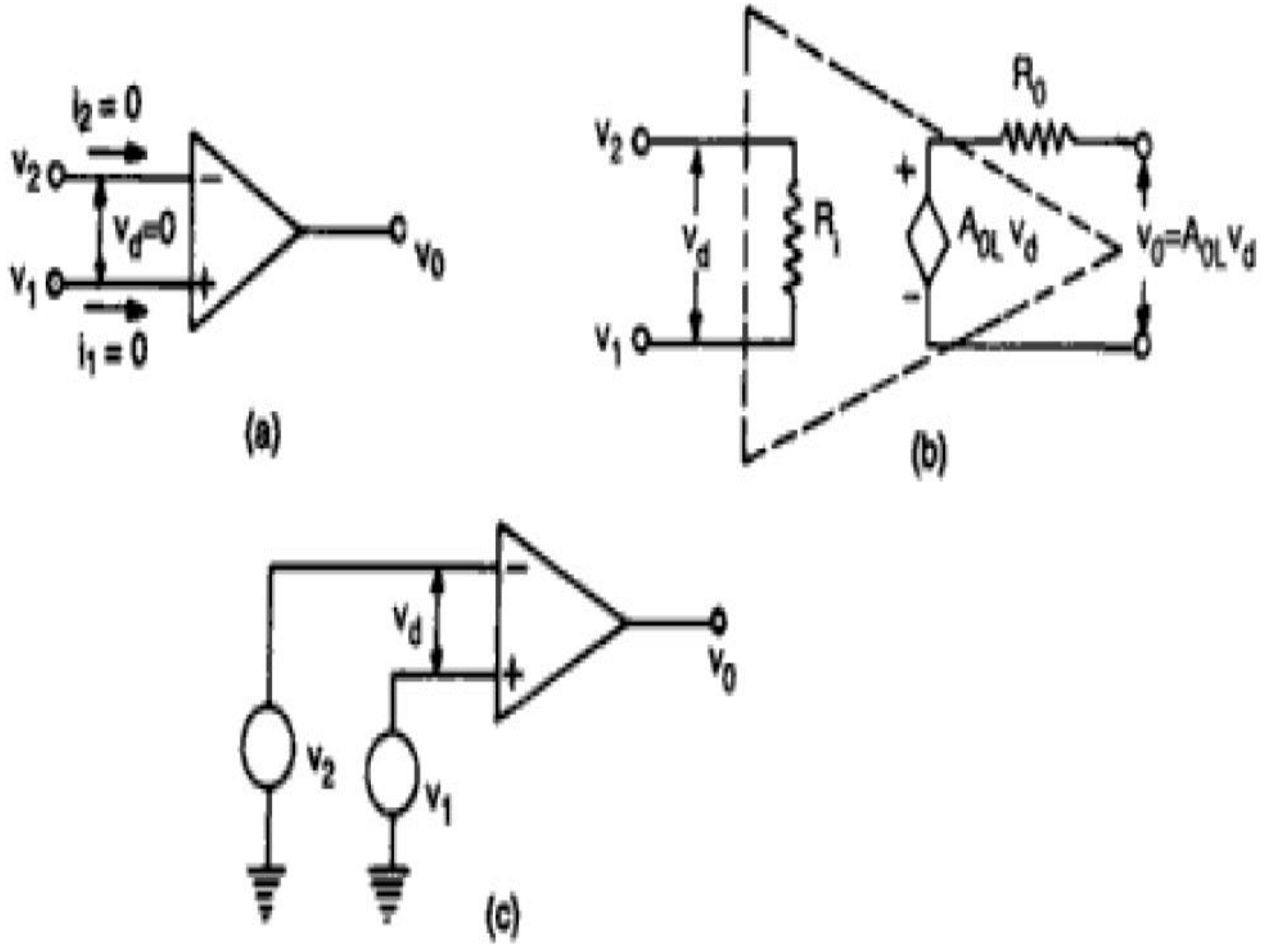


Fig. 2.4 (a) Ideal op-amp (b) Equivalent circuit of an op-amp (c) Open loop circuit

Ideal Characteristics

2.3.1 Open Loop Operation of Op-Amp

The simplest way to use an op-amp is in the open loop mode. Refer to Fig. 2.4 (c) where signals v_1 and v_2 are applied at non-inverting and inverting input terminals respectively. Since the gain is infinite, the output voltage v_o is either at its positive saturation voltage ($+ V_{sat}$) or negative saturation voltage ($-V_{sat}$) as $v_1 > v_2$ or $v_2 > v_1$ respectively. The output assumes one of the two possible output states, that is, $+V_{sat}$ or $-V_{sat}$ and the amplifier acts as a switch only. This has a limited number of applications such as voltage comparator, zero crossing detector etc. which are discussed later.

2.3.2 Feedback in Ideal Op-Amp

The utility of an op-amp can be greatly increased by providing negative feedback. The output in this case is not driven into saturation and the circuit behaves in a linear manner.

- **Close loop configuration**

In close loop configuration , a feedback is introduced

i.e. a part of output is fed back to the input.

The feedback can be of the following two types:

1. **Positive feedback/regenerative feedback**

2. **Negative feedback/degenerative feedback**

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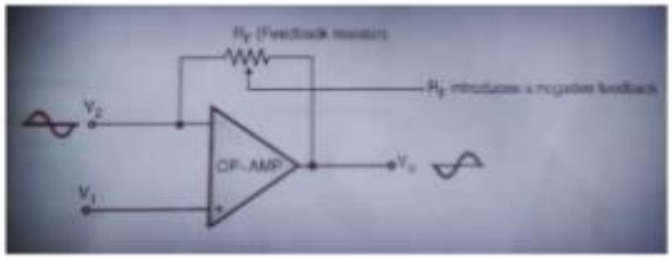
Positive feedback

If the feedback signal and the input signal are in phase with each other then it is called as the positive feedback.

It is used in application such as oscillators and schmitt trigger or regenerative comparators.

Negative feedback



If the signal fed back to the input and the original input signal are 180° out of phase, then it is called as the negative feedback.

In application of op amp as an amplifier, the negative feedback is used.

Advantages of negative feedback

- It stabilizes gain
- Reduces the distortion
- Increases the bandwidth
- Reduces the effect of variations in temperature and supply voltage on the output of op amp

The only disadvantage of negative feedback is low gain

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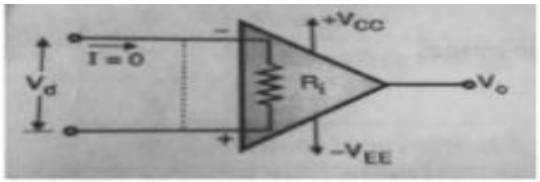
Concept of virtual short

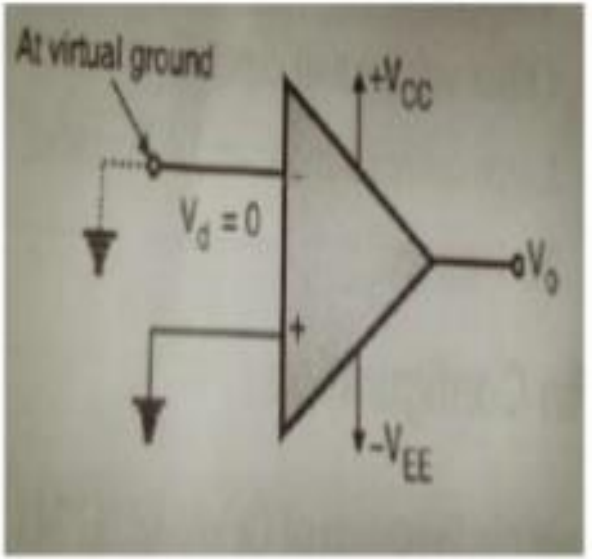
- According to virtual short concept, the potential difference between the two input terminals of an op amp is almost zero.
- In other words both the terminals are approximately at the same potential.



- The input impedance of an OP-AMP is ideally infinite. Hence current flowing from one input terminal to the other will be zero.
- Thus the voltage drop across Ri will be zero and both the terminals will be at the same potential.
- Means they are virtually shorted to each other

Virtual Ground

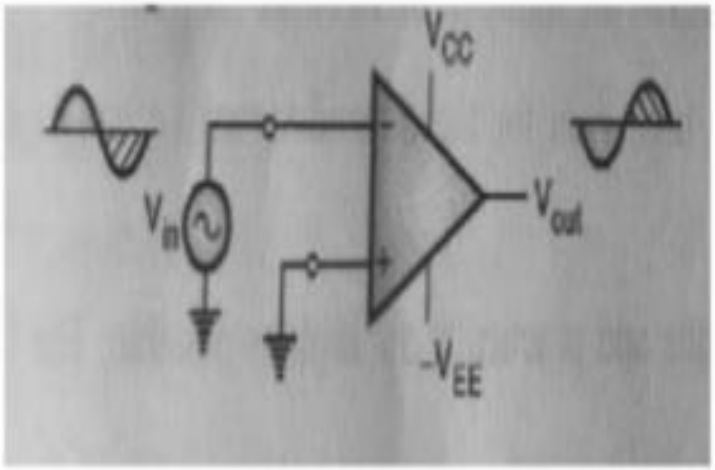
If one of the terminal of OP-AMP is connected to ground then due to the virtual short existing between the other input terminal, the other terminal is said to be at ground potential.

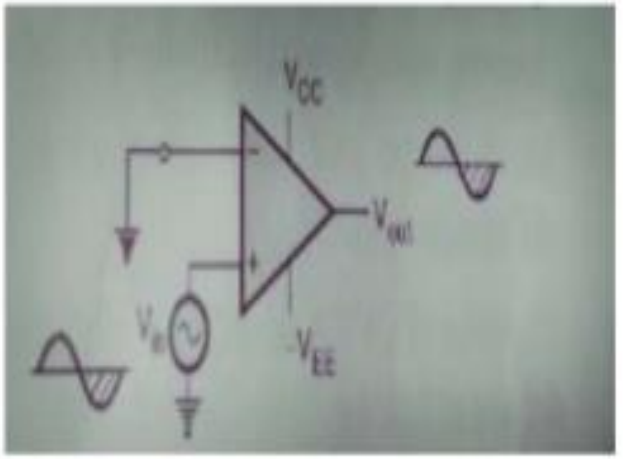


OP-AMP input modes

- **Single ended mode**

  If the input signal is applied to only one of the inputs and the other input terminal is connected to ground it is said to be operating in single ended mode.





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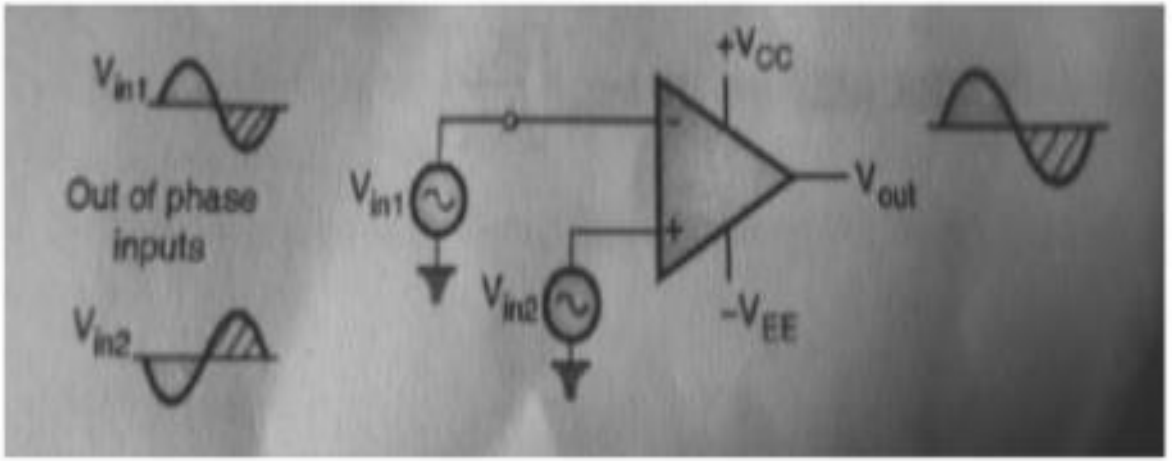
- **Differential mode/double ended**

In differential mode ,two opposite polarity signal are applied to the two inputs of op amp. The difference between the input signal is amplified appears at the output.



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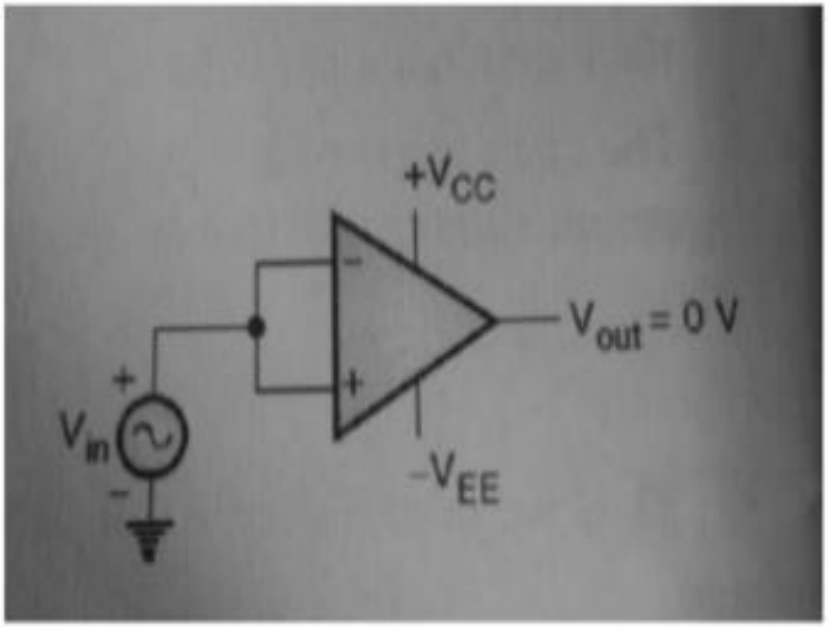
- **Common mode**

  In the common mode of operation, the same input signal is applied to both the input terminals. Ideally a zero voltage should be produced by the op amp.



Non-Ideal Characteristics

DC Characteristics

- Input bias current
- Input offset current
- Input offset voltage
- Thermal drift

AC Characteristics

- Frequency response
- Stability
- Frequency compensation
- Slew rate

DC Characteristics

An ideal op-amp draws no current from the source and its response is also independent of temperature. However, a real op-amp does not work this way. Current is taken from the source into the op-amp inputs. Also the two inputs respond differently to current and voltage due to mismatch in transistors. A real op-amp also shifts its operation with temperature. These non-ideal dc characteristics that add error components to the dc output voltage

Input bias current

The op-amp's input is a differential amplifier, which may be made of BJT or FET. In either case, the input transistors must be biased into their linear region by supplying currents into the bases by the external circuit. In an ideal op-amp, we assumed that no current is drawn from the input terminals. However, practically, input terminals do conduct a small value of dc current to bias the input transistors. The base currents entering into the inverting and non-inverting terminals are shown as I_B^- and I_B^+ respectively in Fig. 3.1 (a). Even though both the transistors are identical, I_B^- and I_B^+ are not exactly equal due to internal imbalances between the two inputs. Manufacturers specify input bias current I_B as the average value of the base currents entering into the terminals of an op-amp.

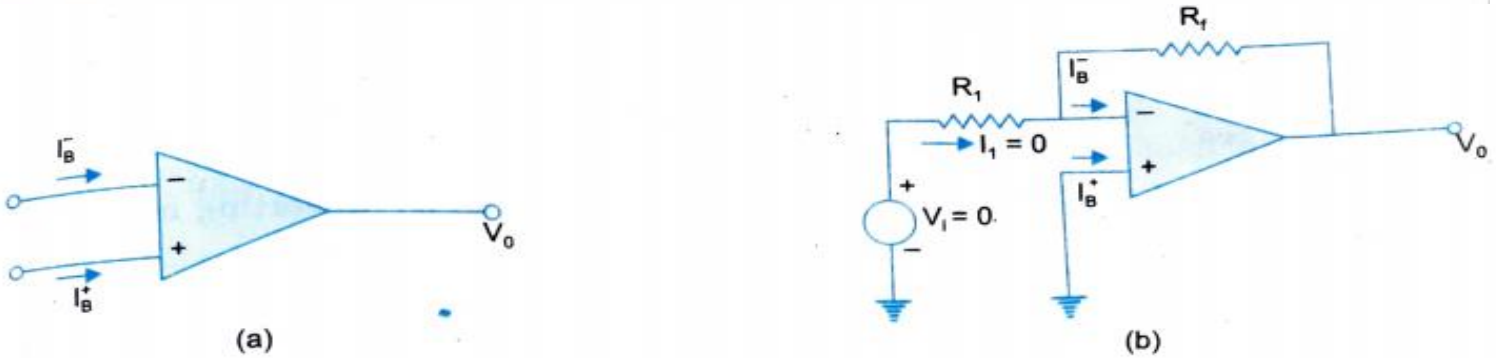


Fig. 3.1 (a) Input bias currents (b) inverting amplifier with bias currents

So,

$$I_B = \frac{I_B^+ + I_B^-}{2} \tag{3.1}$$

Input bias current

For 741, a bipolar op-amp, the bias current is 500 nA or less. The FET input op-amp will have bias currents as low as 50 pA at room temperature.

Consider the basic inverting amplifier of Fig. 3.1 (b). If input voltage V_i is set to zero volt, the output voltage V_o should also be zero volt. Instead, we find that the output voltage is offset by,

$$V_o = (I_B^-)\, R_f \tag{3.2}$$

For a 741 op-amp, with a 1 MΩ feedback resistor,

$$V_o = 500 \text{ nA} \times \text{I M}\Omega = 500 \text{ mV}$$

The output is driven to 500 mV with zero input because of the bias currents. In applications where signal levels are measured in millivolts, this is totally unacceptable. This effect can be compensated for as shown in Fig. 3.1 (c) where a compensation resistor R_{comp} has been added between the noninverting input terminal and ground. Current I_B^+ flowing through the compensating resistor R_{comp} develops a voltage V_1 across it. Then, by KVL, we get,

$$-V_1 + 0 + V_2 - V_o = 0$$

or

$$V_o = V_2 - V_1 \tag{3.3}$$

Input bias current

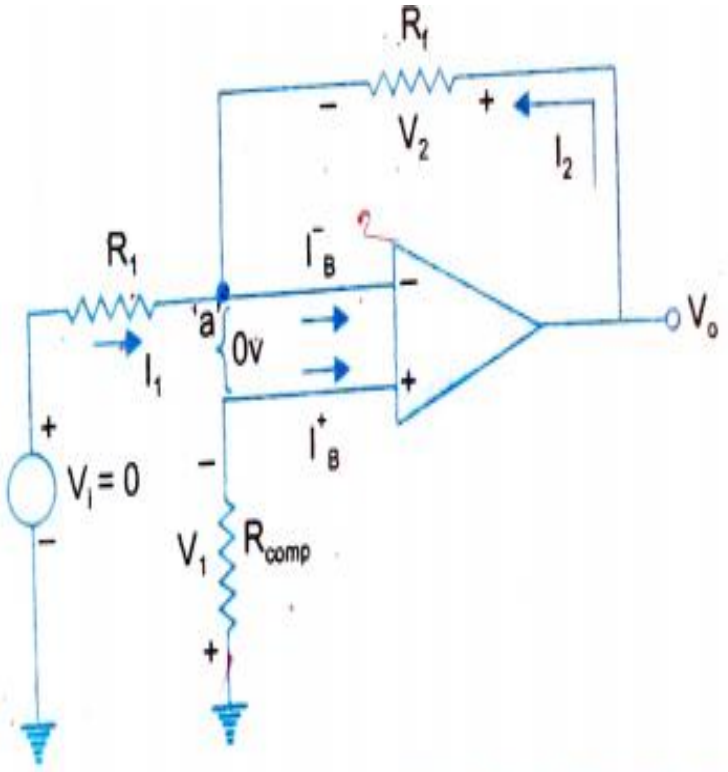


Fig. 3.1 (c) Bias current compensation in an inverting amplifier

By selecting proper value of R_{comp}, V_2 can be cancelled with V_1 and the output V_o will be zero. The value of R_{comp} is derived as

Input bias current

or,
$$R_{comp} = \frac{R_1 R_f}{R_1 + R_f} = R_1 \,||\, R_f$$

that is, to compensate for bias currents, the compensating resistor R_{comp} should be equal to the parallel combination of resistors tied to the inverting input terminal.

The effect of input bias current in a non-inverting amplifier can also be compensated by placing a compensating resistor, R_{comp} in series with the input signal V_i as shown in Fig. 3.1(d).

The value of R_{comp} is again equal to

$$R_{comp} = R_1 \,||\, R_f$$

as the circuits for inverting amplifier and non-inverting amplifier shown in Figs. 3.1(c) and (d) become same with input signal V_i made equal to zero.

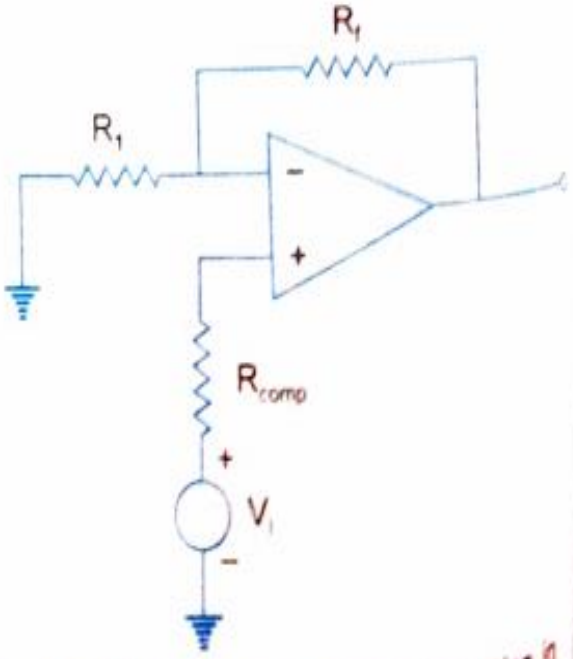


Fig. 3.1 (d) Bias current compensation in a non-inverting amplifier

Input offset current

Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal. Since the input transistors cannot be made identical, there will always be some small difference between I_B^+ and I_B^-. This difference is called the offset current I_{os} and can be written as

$$|I_{os}| = I_B^+ - I_B^- \tag{3.10}$$

The absolute value sign indicates that there is no way to predict which of the bias currents will be larger.

Offset current I_{os} for BJT op-amp is 200 nA and that for FET op-amp is 10 pA. Even with bias current compensation, offset current will produce an output voltage when the input voltage V_i is zero. Referring to Fig. 3.1 (c),

$$V_1 = I_B^+ R_{comp} \tag{3.11}$$

and

$$I_1 = \frac{V_1}{R_1} \tag{3.12}$$

KCL at node 'a' gives,

$$I_2 = (I_B^- - I_1) = I_B^- - \left(I_B^+ \frac{R_{comp}}{R_1} \right) \tag{3.13}$$

Again

$$V_o = I_2 R_f - V_1 = I_2 R_f - I_B^+ R_{comp}$$

$$= \left(I_B^- - I_B^+ \frac{R_{comp}}{R_1} \right) R_f - I_B^+ R_{comp} \tag{3.14}$$

Substituting Eq. (3.9) and after algebraic manipulation,

$$V_o = R_f [I_B^- - I_B^+] \tag{3.15}$$

So,

$$V_o = R_f I_{os} \tag{3.16}$$

Input offset current

So even with bias current compensation and with the feedback resistor of 1 MΩ, a 741 BJT op-amp has an output offset voltage

$$V_o = 1\ \text{M}\Omega \times 200\ \text{nA} = 200\ \text{mV}$$

with a zero input voltage. It can be seen from Eq. (3.16) that the effect of offset current can be minimized by keeping feedback resistance small.

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Input offset voltage

Inspite of the use of the above compensating techniques, it is found that the output voltage may still not be zero with zero input voltage. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminals to make output voltage zero. This voltage is called input offset voltage V_{ios}. This is the voltage required to be applied at the input for making output voltage to zero volts as shown in Fig. 3.2. (a).

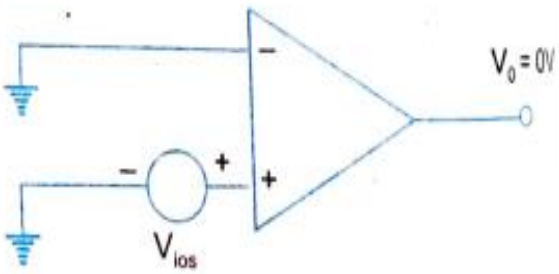


Fig. 3.2 (a) Op-amp showing input offset voltage

Let us now examine the effect of V_{ios} on the output of a non-inverting and inverting op-amp amplifier as shown in Fig. 3.2 (b, c). If V_i is set to zero, the circuits of Fig. 3.2 (b and c) become the same as in Fig. 3.2 (d). The voltage V_2 at the (–) input terminal is given by

$$V_2 = \left(\frac{R_1}{R_1 + R_f}\right) V_o \qquad (3.20$$

$V_o = V_2 \dfrac{R_1 + R_f}{R_1}$

or $= V_2\left(1 + \dfrac{R_f}{R_1}\right)$

$$V_o = \left(\frac{R_1 + R_f}{R_1}\right) V_2 = \left(1 + \frac{R_f}{R_1}\right) V_2 \qquad (3.2$$

Since, $V_{ios} = |V_i - V_2|$ and $V_i = 0$,

Input offset voltage

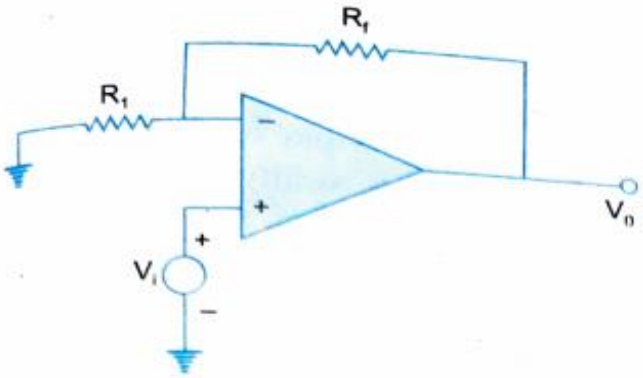


Fig. 3.2 (b) Non-inverting amplifier

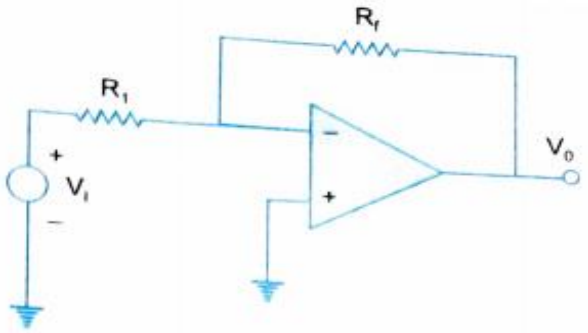


Fig. 3.2 (c) Inverting amplifier

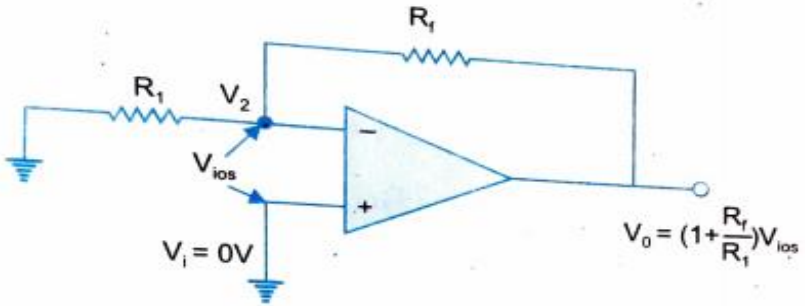


Fig. 3.2 (d) equivalent circuit for $V_i = 0$

$$V_{ios} = |0 - V_2| = V_2 \tag{3.22}$$

or,

$$\boxed{V_o = \left(1 + \frac{R_f}{R_1}\right) V_{ios}} \tag{3.23}$$

Thermal drift

Bias current, offset current and offset voltage change with temperature. A circuit carefully nulled at 25°C may not remain so when the temperature rises to 35°C. This is called drift. Often, offset current drift is expressed in nA/°C and offset voltage drift in mV/°C. These indicate the change in offset for each degree celsius change in temperature.

There are very few circuit techniques that can be used to minimize the effect of drift. Careful printed circuit board layout must be used to keep op-amps away from source of heat. Forced air cooling may be used to stabilize the ambient temperature.

Slew rate

The rise time of an amplifier is defined as the time the output takes to change from 10 to 90 percent of the final value for a step input and is given as 0.35/BW, where BW is the bandwidth of the amplifier. Ideal response time should be zero second as BW is infinite for ideal op-amp, that is, output voltage should respond instantaneously to any change in the input. Rise time is usually specified for small signals, usually when the peak output voltage is less than one volt. However, for large signal output (i.e., $V_m > 1$ volt), the op-amp's speed is limited by slew rate, Manufacturers specify slew rate that gives the circuit designer a good idea of how quickly a given op-amp responds to changes of input voltage. An op-amp's slew rate is related to its frequency response. Usually op-amps with wide bandwidth will have higher (better) slew rates.

The slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage and is usually specified in V/μs. For example, a 1V/μs slew rate means that the output rises or falls by 1 V in one microsecond. An ideal slew rate is infinite which means that op-amp's output voltage should change instantaneously in response to input step voltage. Practical IC op-amps have specified slew rates from 0.1 V/μs to well above 1000 V/μs. Slew rate listed in the data sheet is usually specified for unity gain and no load. The slew rate improves with higher closed loop gain and dc supply voltage. It is also a function to termperature and generally decreases with an increase in temperature.

Slew rate

What causes slew rate? There is usually a capacitor within or outside an op-amp to prevent oscillation. It is this capacitor which prevents the output voltage from responding immediately to a fast changing input. The rate at which the voltage across the capacitor v_c increases is given by,

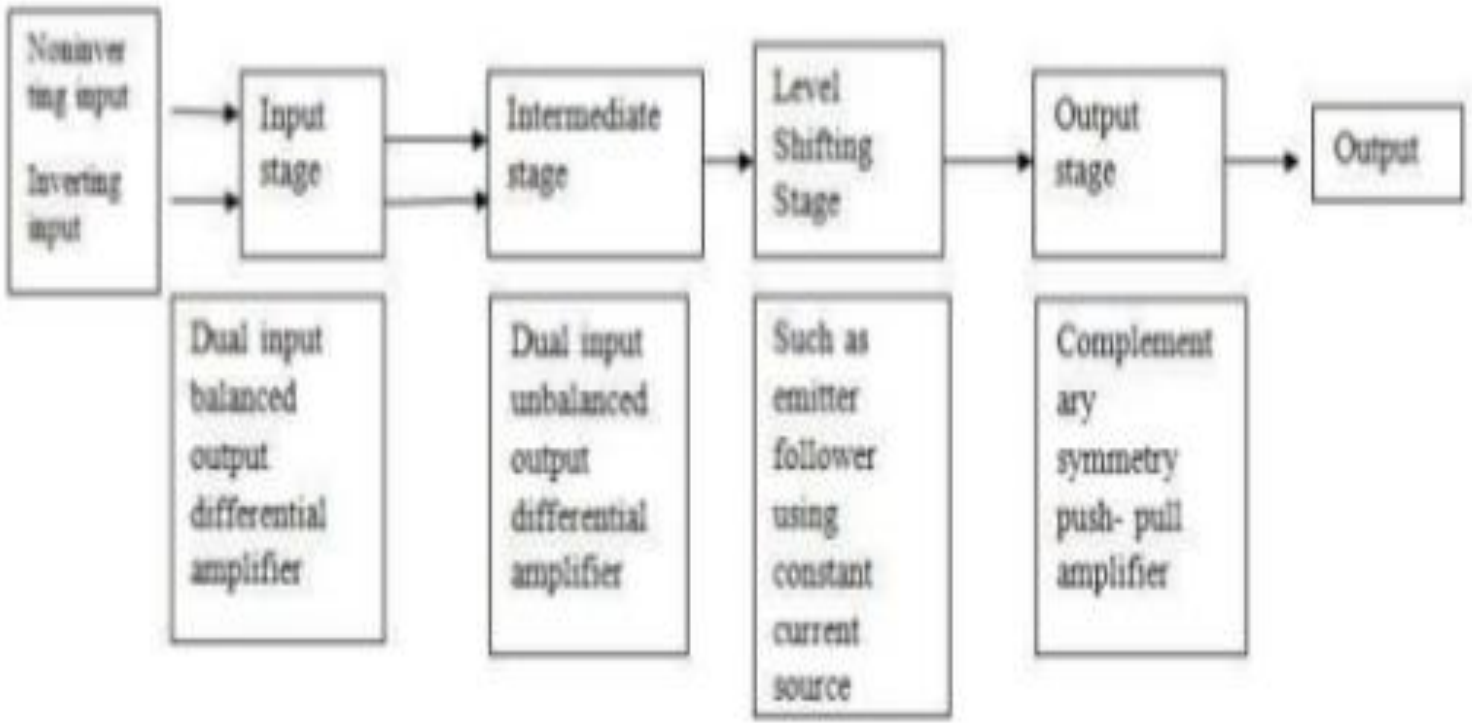
$$\frac{dv_c}{dt} = \frac{I}{C} \tag{3.49}$$

Here, I is the maximum current furnished by op-amp to the capacitor C. This means that for obtaining faster slew rate, op-amp should have either a higher current or a small compensating capacitor. For the 741 C, the maximum internal capacitor charging current is limited to about 15 μA. So the slew rate (SR) of 741 C is,

$$SR = \left.\frac{dv_c}{dt}\right|_{max} = \frac{I_{max}}{C} = \frac{15\,\mu A}{30\,pF} = 0.5\ V/\mu s$$

Slew rate limits the response speed of all large signal waveshapes.

Internal Structure



Internal Structure

- **Input stage** provides most of the voltage gain of OP-AMP and decides input resistance.
- **Intermediate stage** is another differential amplifier which is driven by the output of input stage.
- Due to direct coupling between the first two stages, the input of level shifting is an amplified signal with some non zero dc level. **Level shifting stage** is used to bring this dc level to zero volts with respect to ground.
- **Output stage** increase the current supplying capability of OP-AMP and also provides low output resistance.

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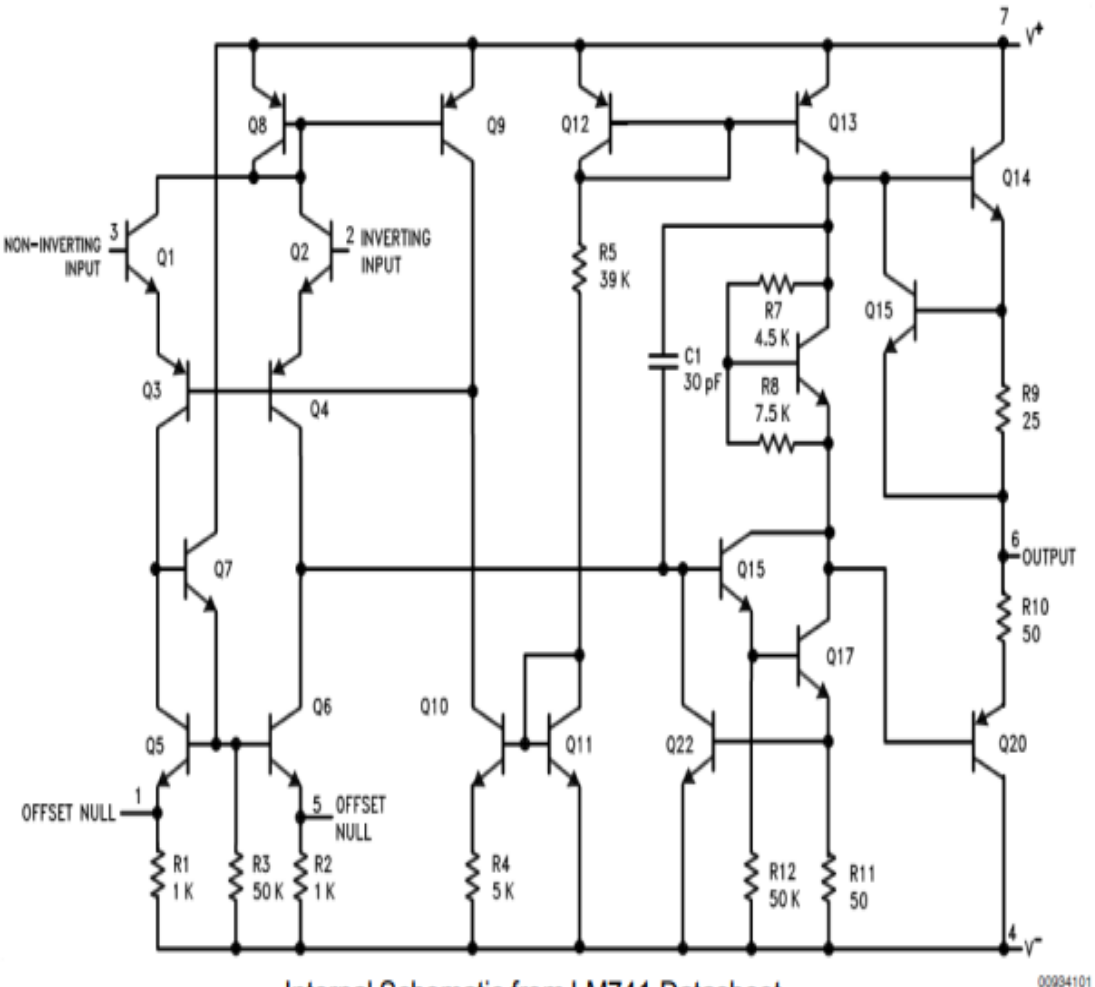
Internal Structure

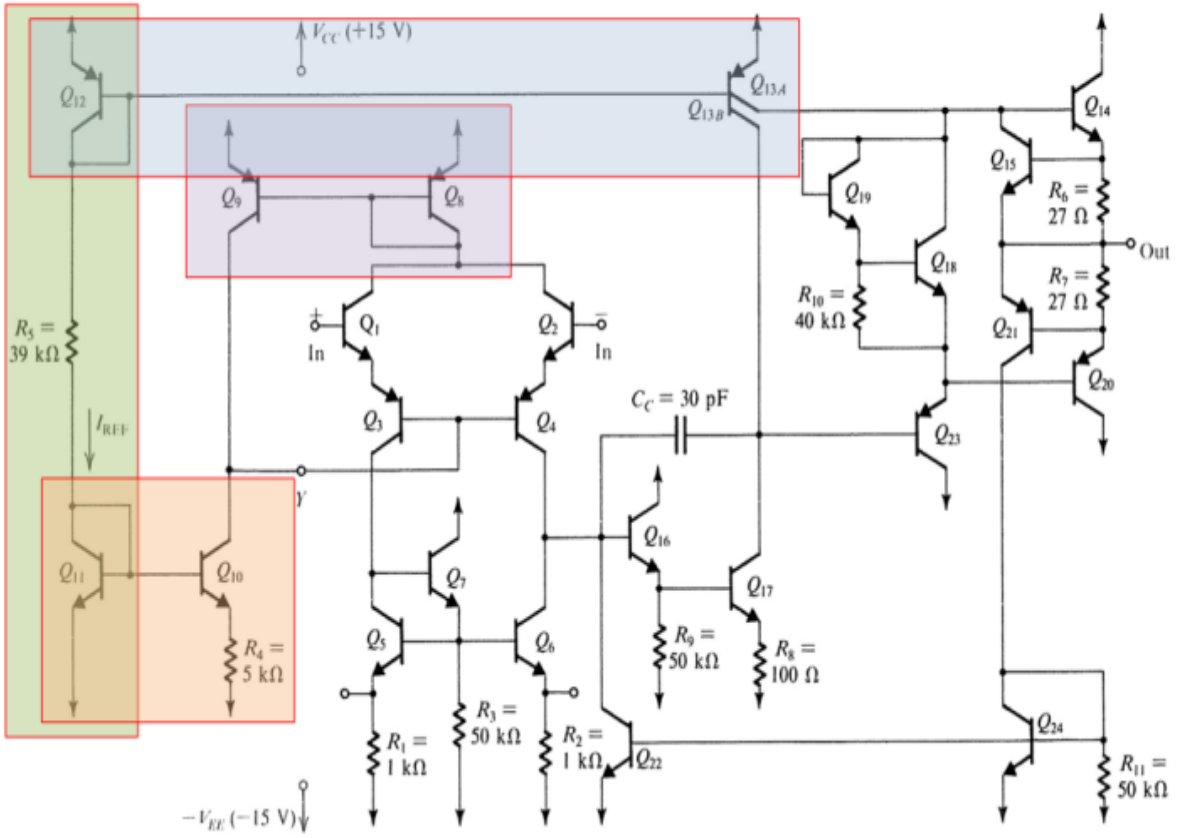
µA741 Op-Amp

- Bias Circuit
- Input Stage
- Intermediate Stage
- Output Stage
- Short-circuit Protection

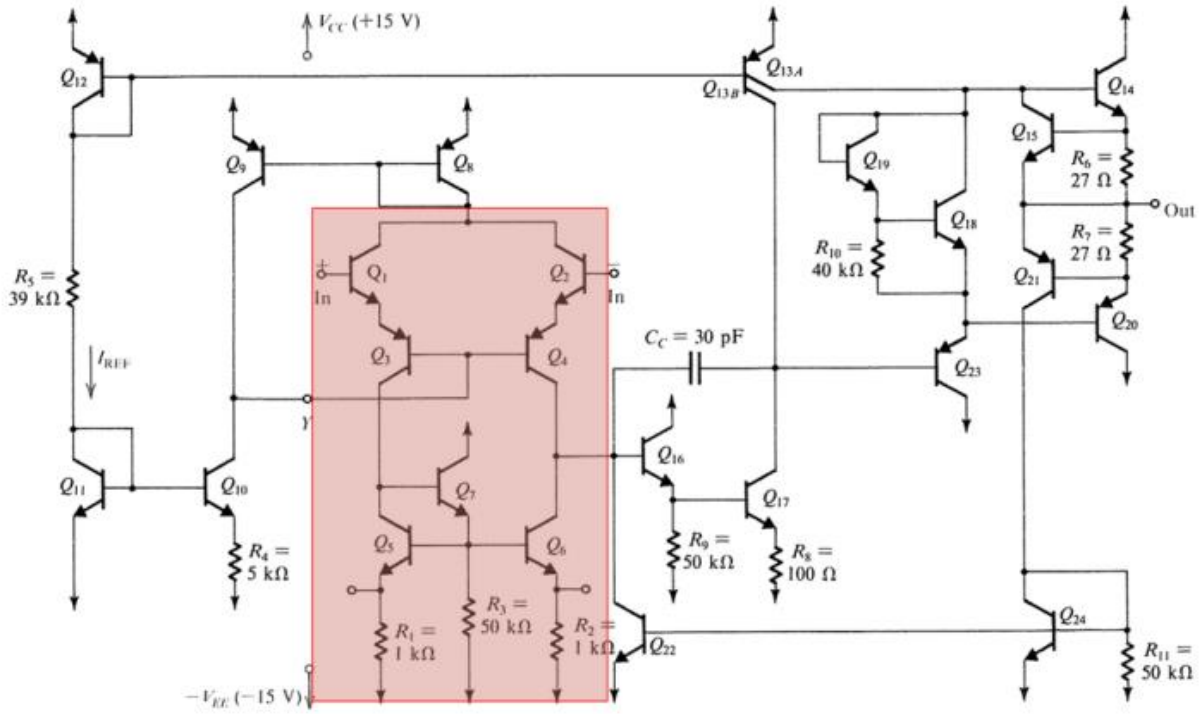


Internal Schematic from LM741 Datasheet

Biasing Circuit



Input Stage

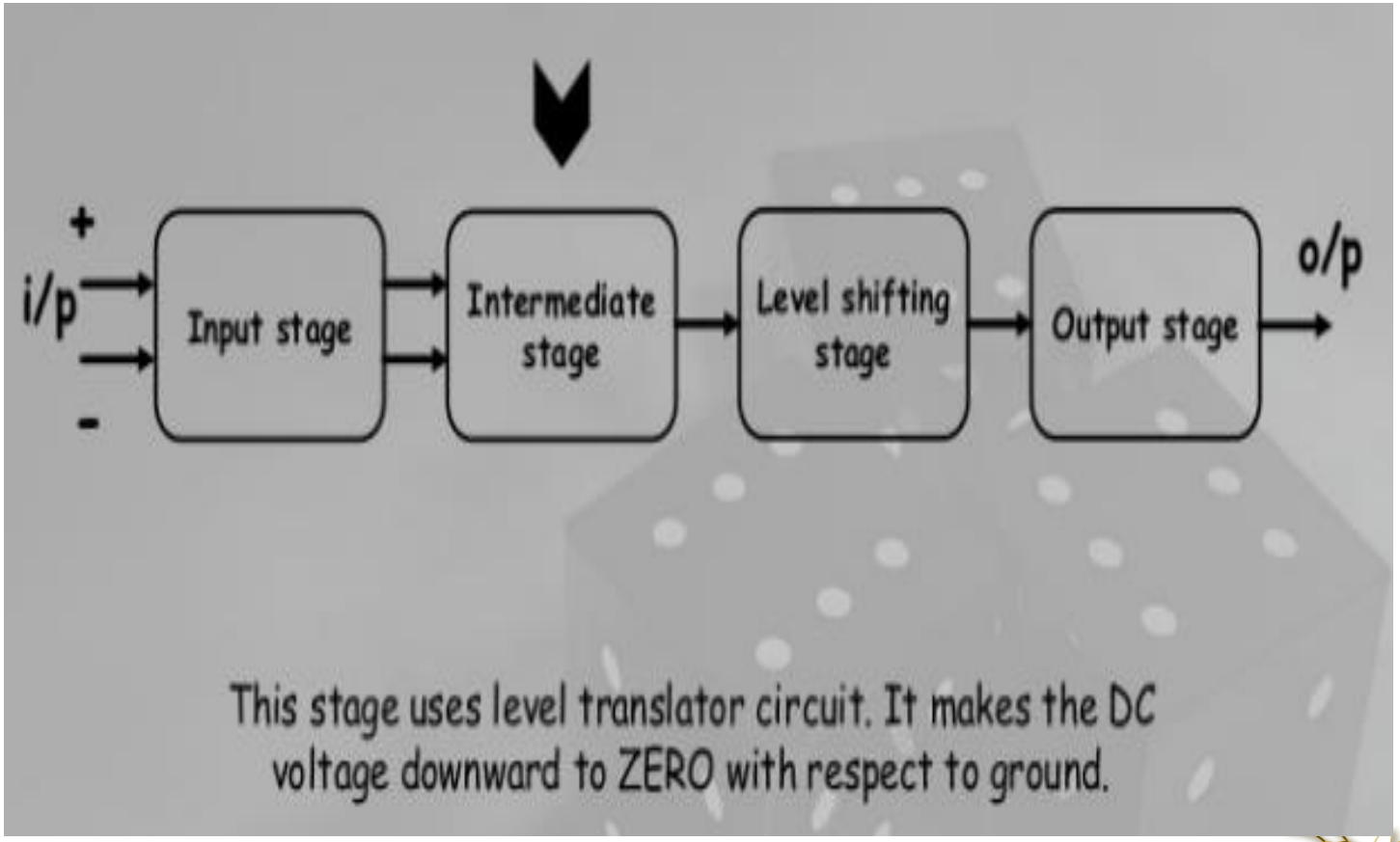


Input Stage

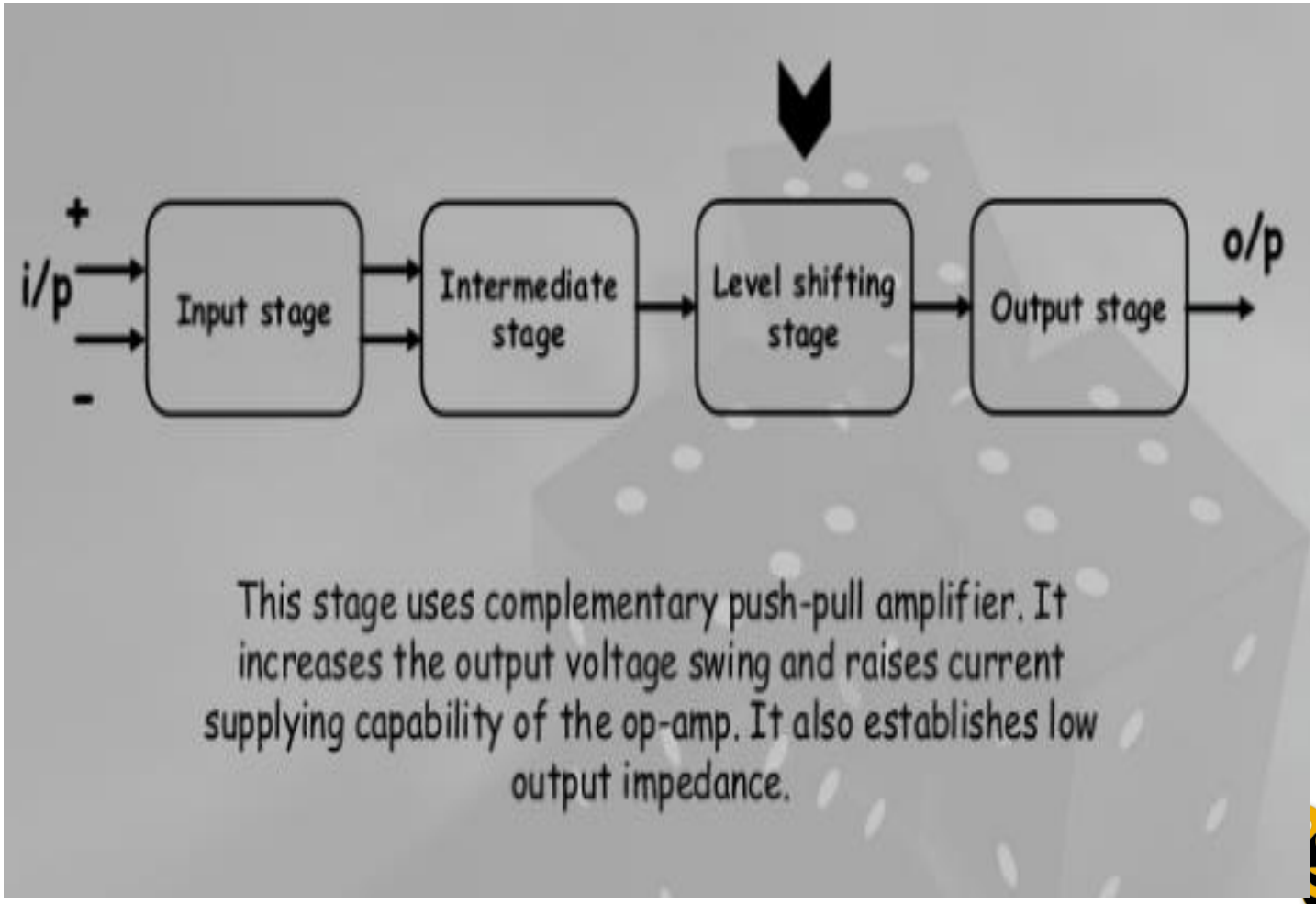
- Q1, Q2 are emitter followers.
- Q3, Q4 in common-base configuration serve as differential amplifier, level shifters and protect Q1, Q2 against emitter-base junction breakdown.
- Q5, Q6, Q7 and R1, R2, R3 provide the load (active load) for the differential amplifier.

Georgia Tech

Intermediate stage

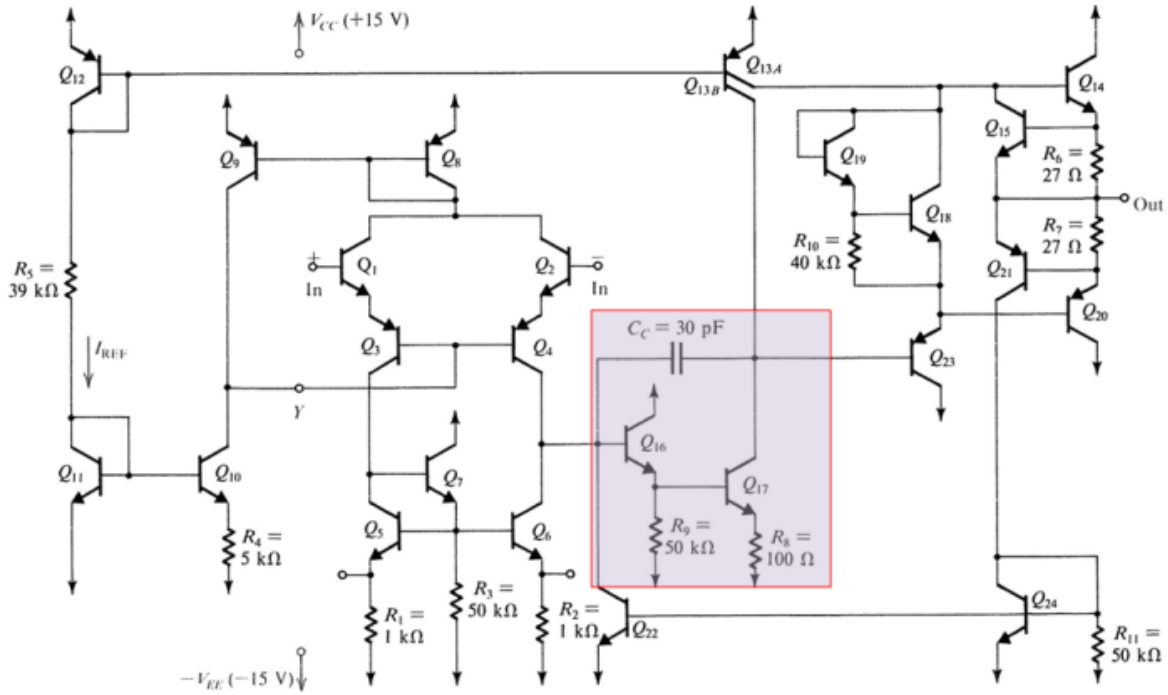


Level Shifting Stage



This stage uses complementary push-pull amplifier. It increases the output voltage swing and raises current supplying capability of the op-amp. It also establishes low output impedance.

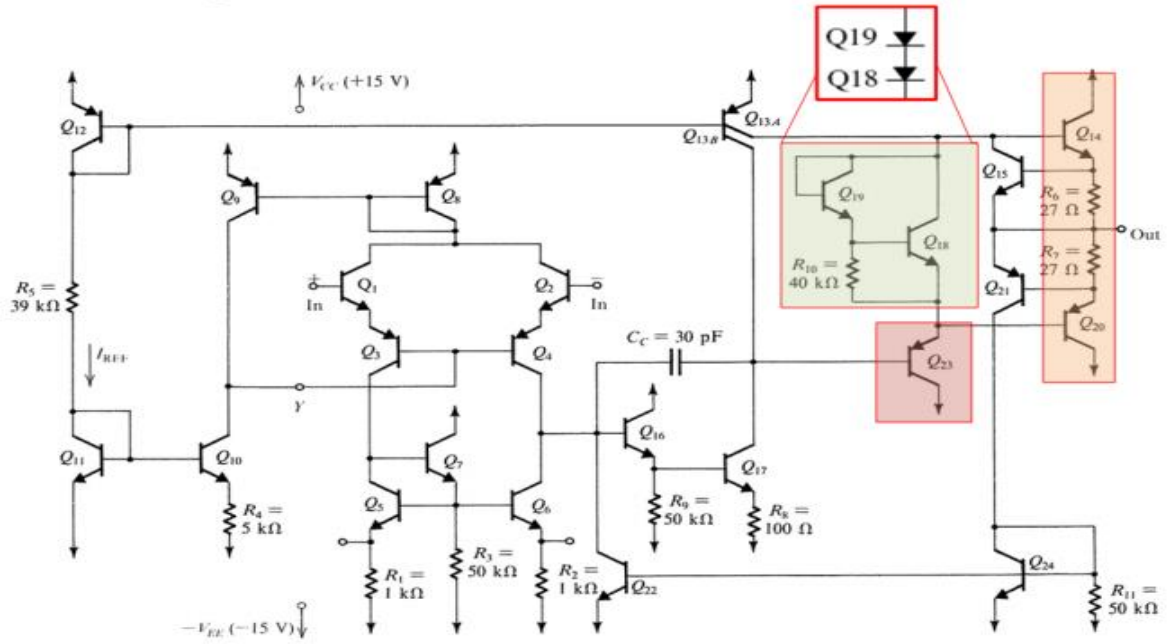
Intermediate Stage



Intermediate Stage

- Q16 is an emitter follower.
- Q17 is a common-emitter amplifier, loaded by Q13B.
  - GAIN≈ $(g_{m\text{-}Q17})(r_{0\text{-}Q13B})$
- Cc is the internal compensation cap used to maintain stability when the op-amp is used in a feedback configuration.

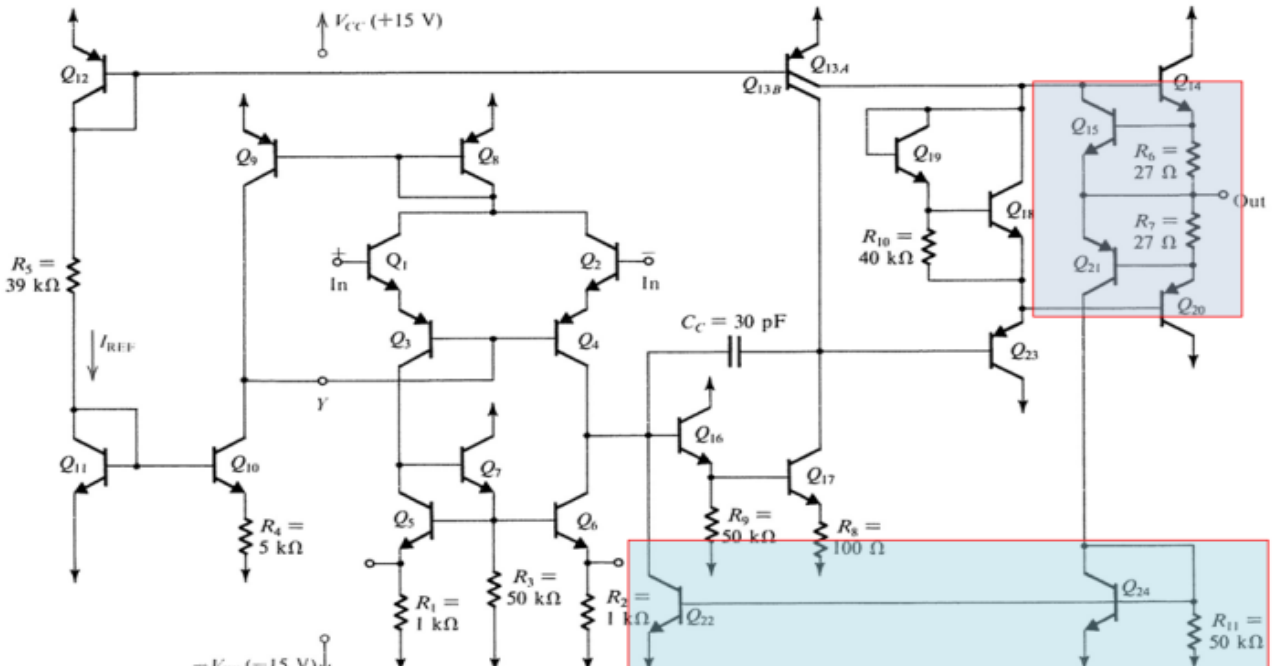
Output Stage



Output Stage

- Q23 is an emitter follower.
- Q14, Q20 are a complementary push-pull, or Class AB amplifier.
- Q19, Q18 are a Darlington-pair, but act similar to diodes. They maintain a V_{BE} drop to smooth out the crossover distortion of Q14, Q20.

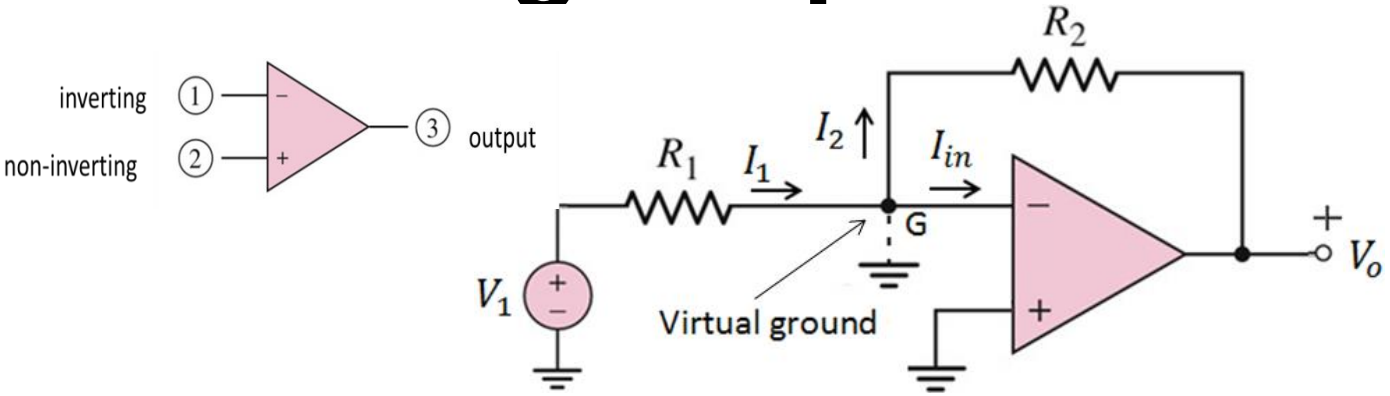
Short-circuit Protection



Short-circuit Protection

- Q15, Q21 are normally off.
- If too much current is being output (~25mA), the voltage drop across R6, R7 will turn Q15, Q21 on to bleed off the current via Q22, Q24 current mirror.

Inverting Amplifier



Op-amp as an inverting amplifier

Voltage at node 1 (inverting) = voltage at node 2 (non-inverting) KCL at node 1:

$I_1 - I_2 - I_{in} = 0$

$(V_i - 0) / R_1 = (0 - V_o) / R_2$

$V_i / R_1 = - V_o / R_2$

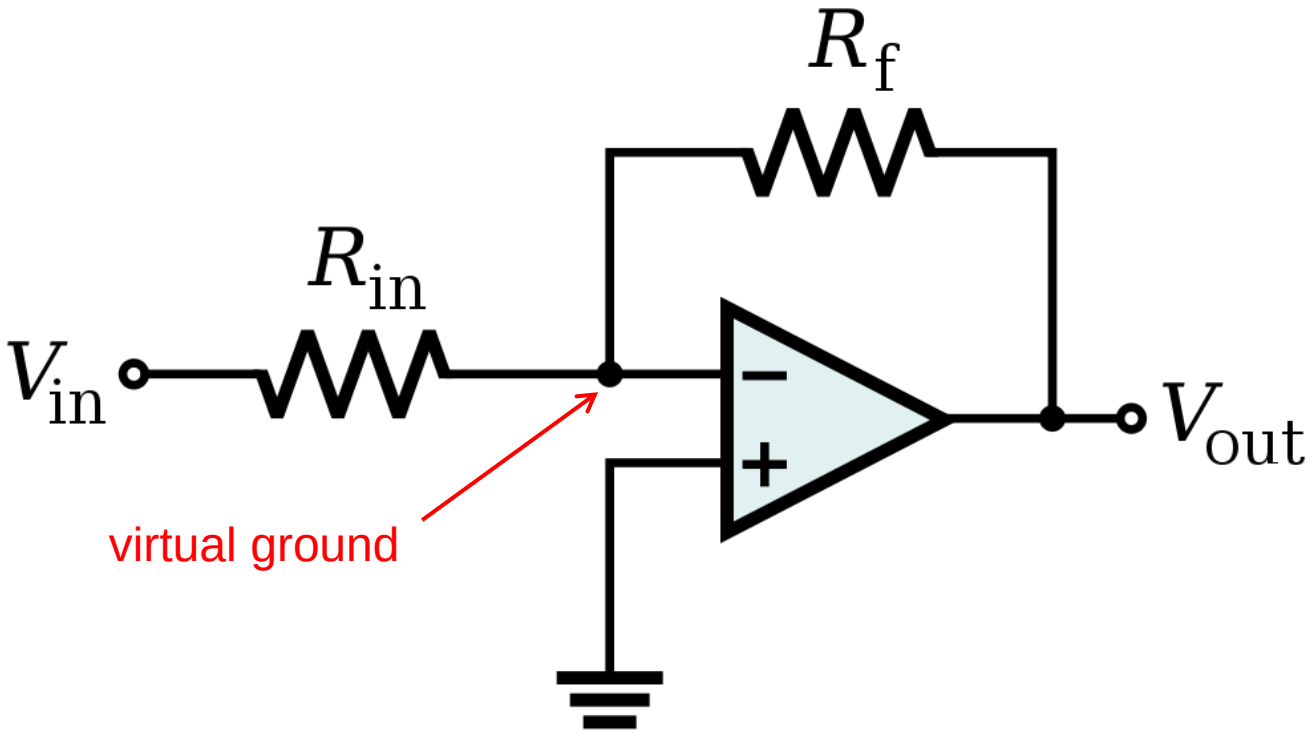
$$\frac{V_o}{V_i} = -\frac{R_2}{R_1}$$

Voltage gain, $A_v = \frac{V_0}{V_i} = -\frac{R_2}{R_1}$

Input Resistance, $R_i = \frac{V_i}{I_1} = R_1$

Output resistance, $R_o = \frac{V_o}{I_2} = R_2$

Inverting Amplifier Analysis



$$V_{out} = -\frac{R_f}{R_{in}} V_{in}$$

Non - Inverting Amplifier

Voltage at node 1 (inverting) = voltage at node 2 (non-inverting) KCL at node 1:

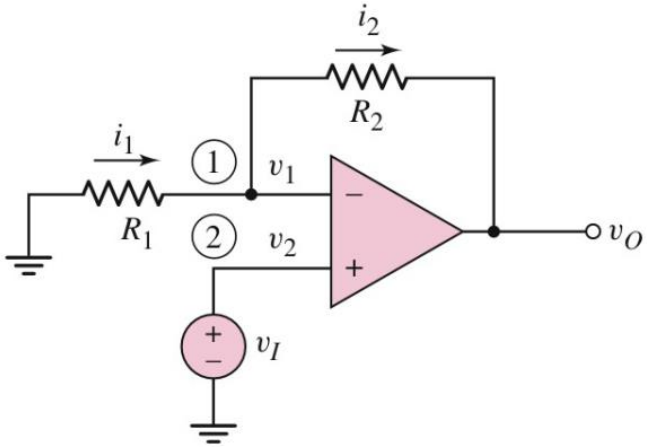
$i_1 - i_2 = 0$

$(0 - V_i) / R_1 = (V_i - V_o) / R_2$

$-(V_i / R_1) = (V_i / R_2) - (V_o / R_2)$

$$V_o / R_2 = (V_i / R_2) + (V_i / R_1) = V_i \left(\frac{1}{R_2} + \frac{1}{R_1} \right)$$

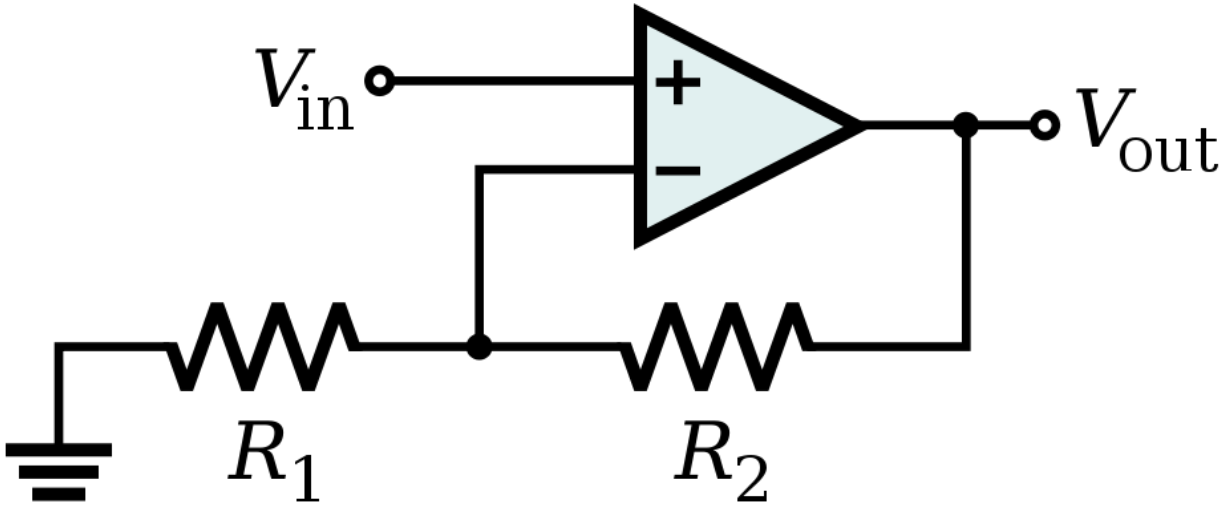
$$V_o / V_i = R_2 \left(\frac{1}{R_2} + \frac{1}{R_1} \right)$$



Noninverting amplifier

Voltage gain, $$A_v = \frac{V_0}{V_i} = 1 + \frac{R_2}{R_1}$$

Non-Inverting Amplifier Analysis



$$V_{\text{out}} = V_{\text{in}} \left(1 + \frac{R_2}{R_1}\right)$$

Mathematics of the Op-Amp

- The gain of the Op-Amp itself is calculated as:

$$G = V_{out}/(V_+ - V_-)$$

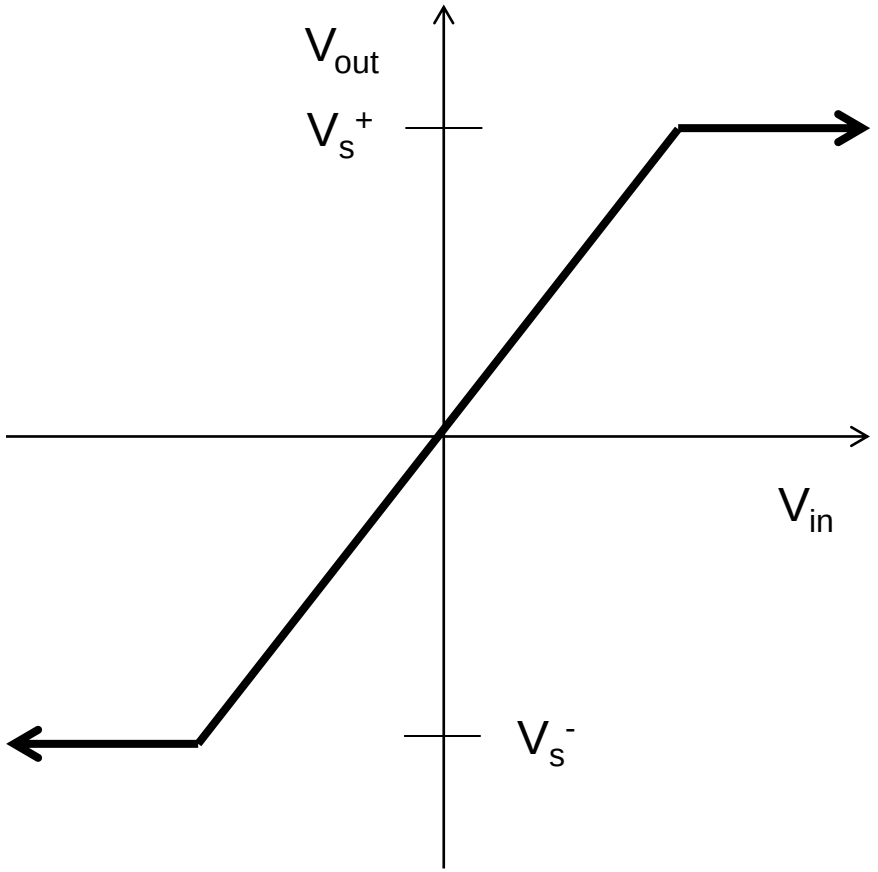
- The maximum output is the power supply voltage

- When used in a circuit, the gain of the circuit (as opposed to the op-amp component) is:

$$A_v = V_{out}/V_{in}$$

Op-Amp Saturation

- As mentioned earlier, the maximum output value is the **supply voltage**, positive and negative.
- The gain (G) is the slope between saturation points.



Differentiator

When the inverting input terminal resistor of an op-amp inverter circuit is replaced by a capacitor the circuit is worked as a differentiator circuit.

Applying KCL at node point G

$I_S - I_{in} - I_2 = 0$

$I_{in} = 0$ since, $R_{in} = \infty$

Therefore, $I_2 = I_S$

Since G point is a virtual ground

Voltage across the capacitor,

$$V_C = \frac{Q}{C} = V_S$$

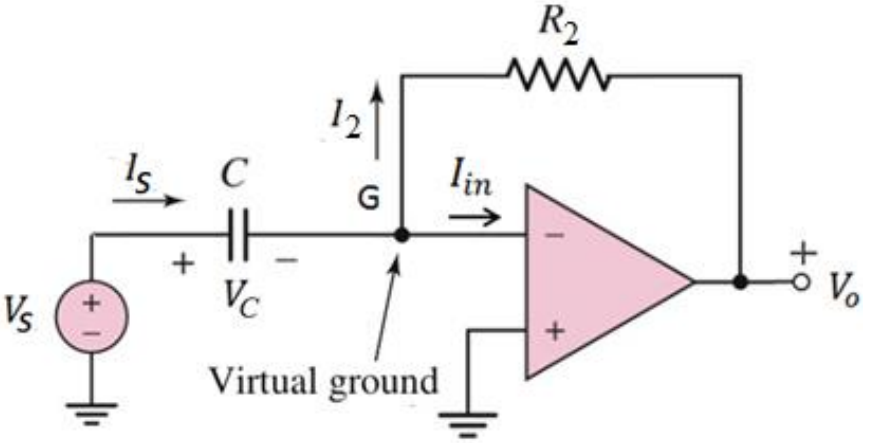
Or, $$I_S = \frac{dQ}{dt} = C\frac{dV_S}{dt}$$

Because $Q = CV_S$

Again, the output voltage,

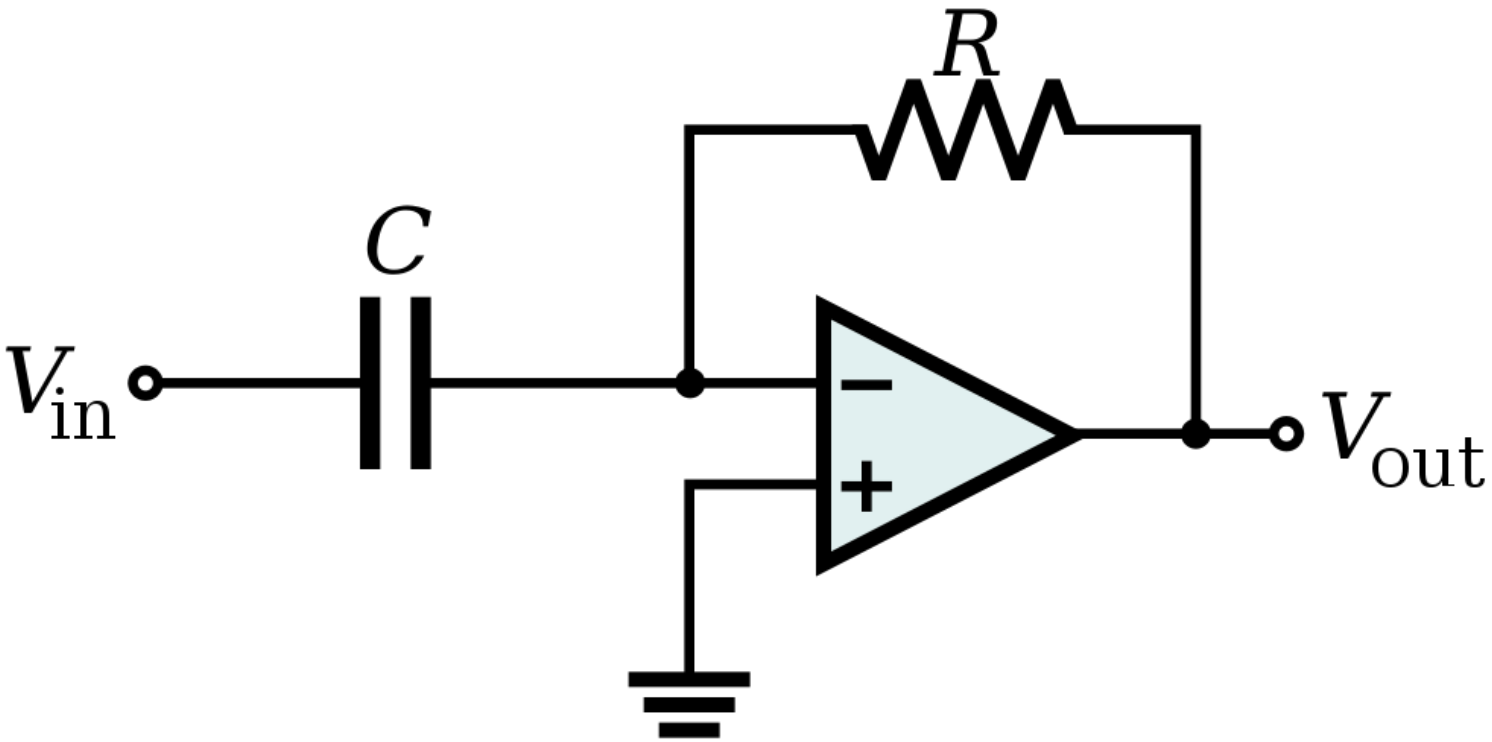
$V_o = -I_2 R_2 = -I_S R_2$

Therefore, $$V_o = -CR_2\frac{dV_S}{dt}$$



Differentiator circuit

Op-Amp Differentiator



$$V_{out} = -RC\frac{dV_{in}}{dt}$$

Integrator

When the feedback resistor of an inverter circuit is replaced by a capacitor the circuit is worked as an integrator circuit -cause the output to respond to changes in the input voltage over time

Applying KCL at node point G

$I_S - I_{in} - I_C = 0$

$I_{in} = 0$ since, $R_{in} = \infty$

Since G point is a virtual ground

$$I_S = I_C = \frac{V_S}{R_1}$$

Again, the voltage across the capacitor,

$$V_C = \frac{Q}{C} = -V_o$$

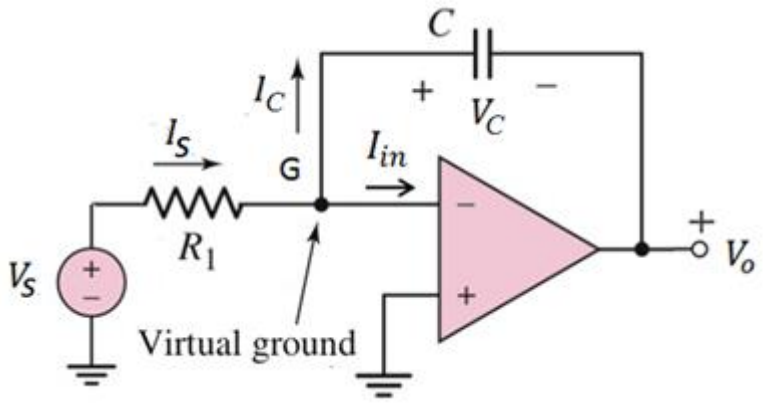
But the capacitor charge,

$$Q = \int I_S \, dt = \int \frac{V_S}{R_1} dt$$

Output voltage, $$V_o = \frac{-1}{R_1 C} \int V_S \, dt$$

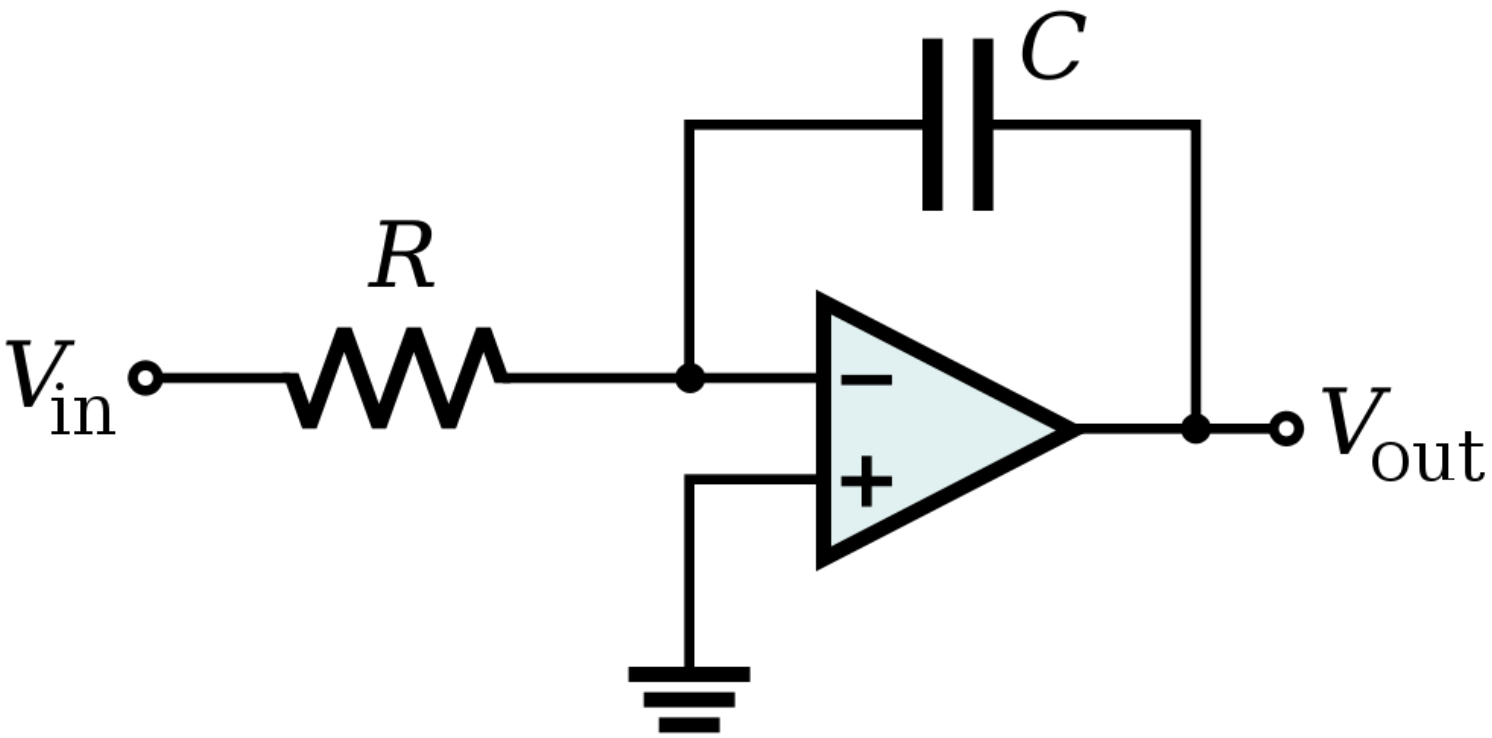
If the capacitor has some initially voltage, V_x

$$V_o = V_x - \frac{1}{R_1 C} \int V_S \, dt$$



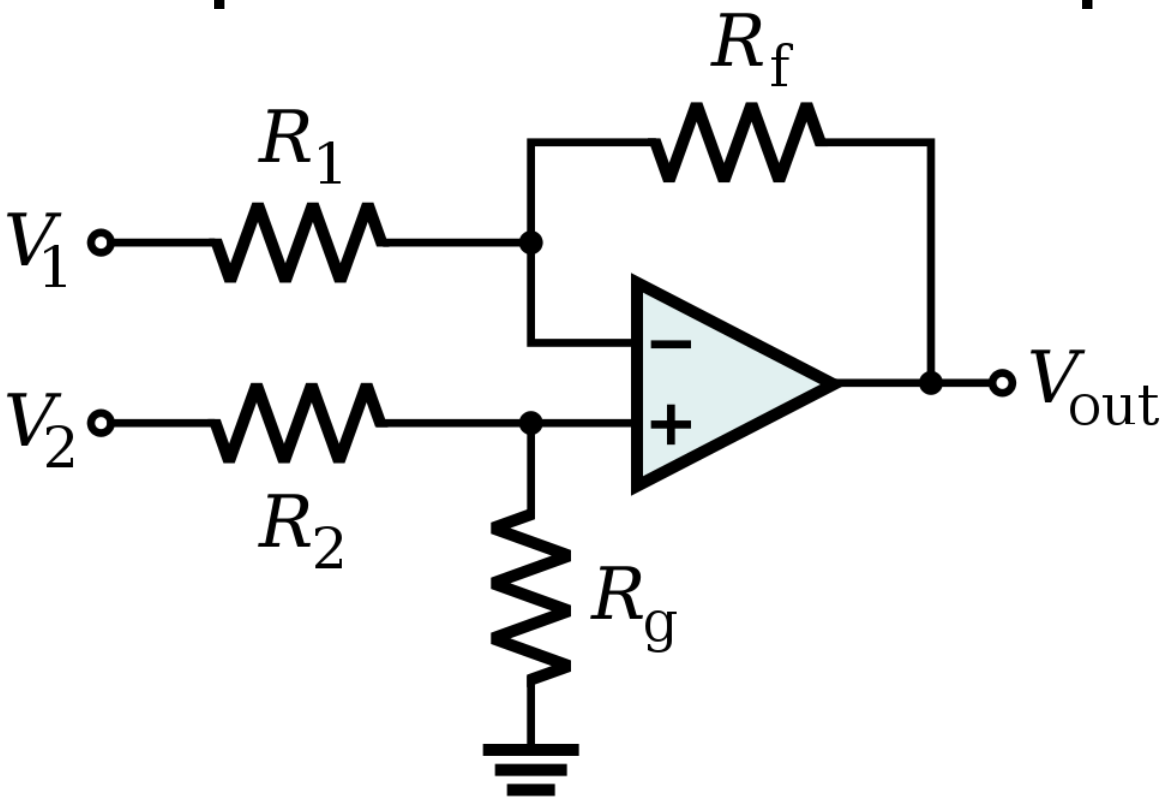
Integrator circuit

Op-Amp Integrator



$$V_{out} = -\int_0^t \frac{V_{in}}{RC}\,dt + V_{initial}$$

Op-Amp Differential Amplifier



$$V_{out} = \frac{(R_f + R_1)\,R_g}{(R_g + R_2)\,R_1} V_2 - \frac{R_f}{R_1} V_1$$

If $R_1 = R_2$ and $R_f = R_g$: $V_{out} = \frac{R_f}{R_1}(V_2 - V_1)$

Introduction

- Filters are circuits that are capable of *passing signals within a band* of frequencies while *rejecting or blocking* signals of frequencies *outside this band*. This property of filters is also called "frequency selectivity".
- Filter can be passive or active filter.

Passive filters: The circuits built using RC, RL, or RLC circuits.

Active filters : The circuits that employ one or more op-amps in the design an addition to resistors and capacitors

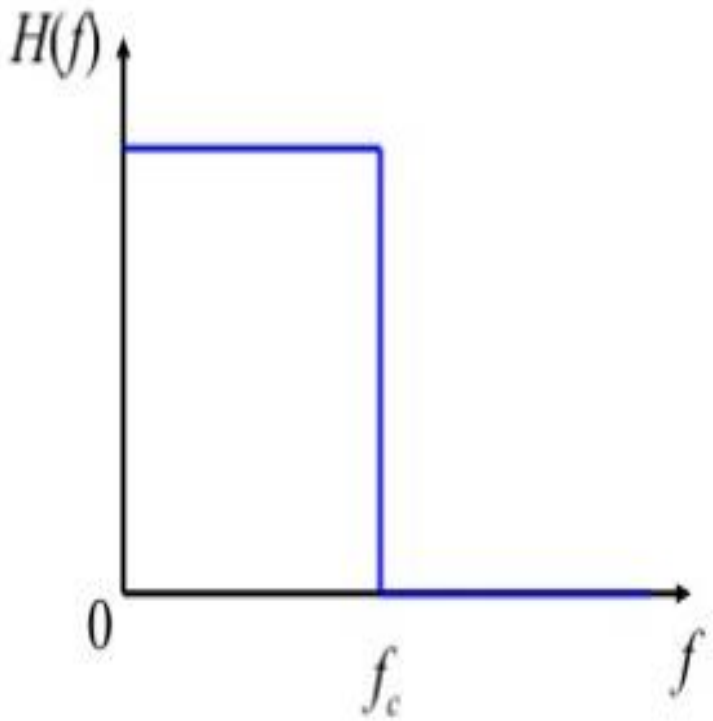
Active Filters

- **Active Filters** contain active components such as operational amplifiers, transistors or FET's within their circuit design. They draw their power from an external power source and use it to boost or amplify the output signal.
- Filter amplification can also be used to either shape or alter the frequency response of the filter circuit by producing a more selective output response, making the output bandwidth of the filter more narrower or even wider. Then the main difference between a "passive filter" and an "active filter" is amplification.

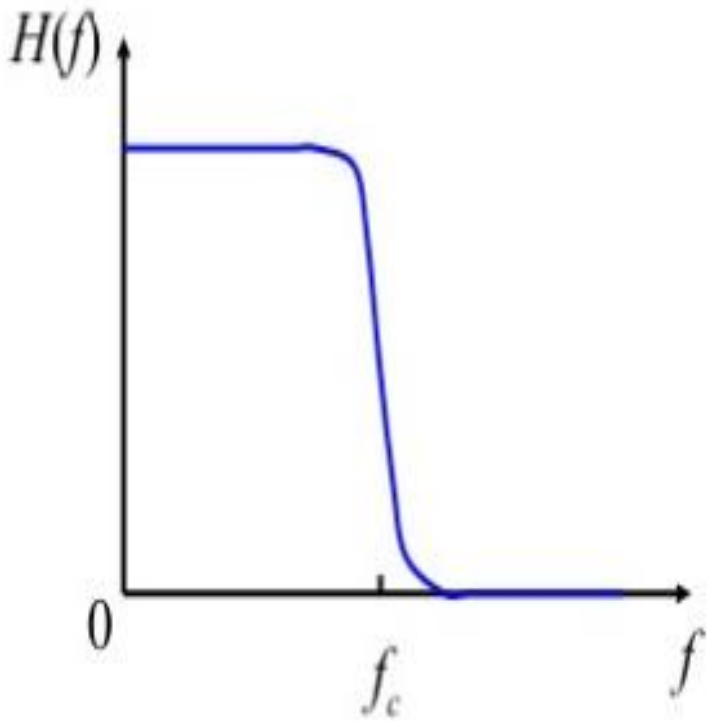
Types of Filters

- There are two broad categories of filters:
  - An *analog filter* processes continuous-time signals
  - A *digital filter* processes discrete-time signals.
- The analog or digital filters can be subdivided into four categories:
  - Low pass Filters
  - High pass Filters
  - Band stop Filters
  - Band pass Filters

Filter Response

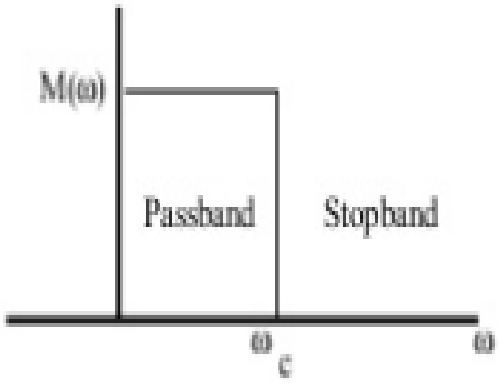


Ideal "brick wall" filter

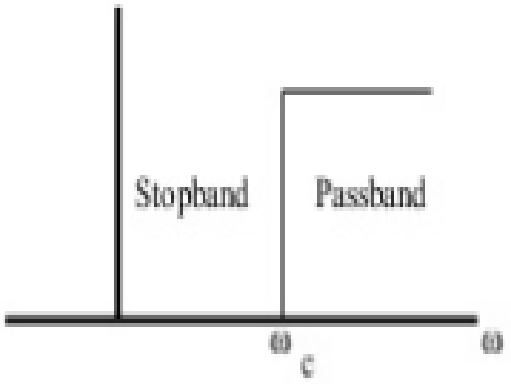


Practical filter

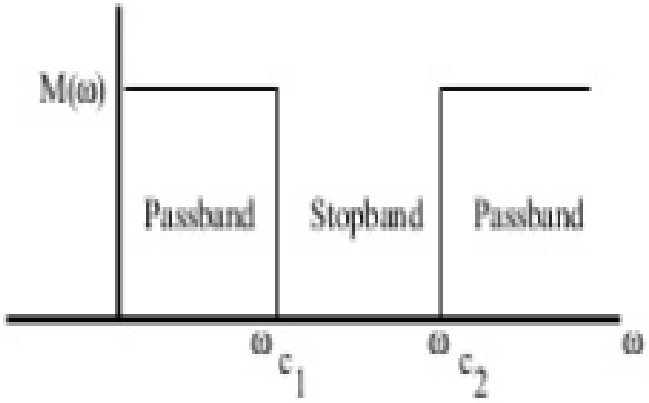
Lowpass Filter



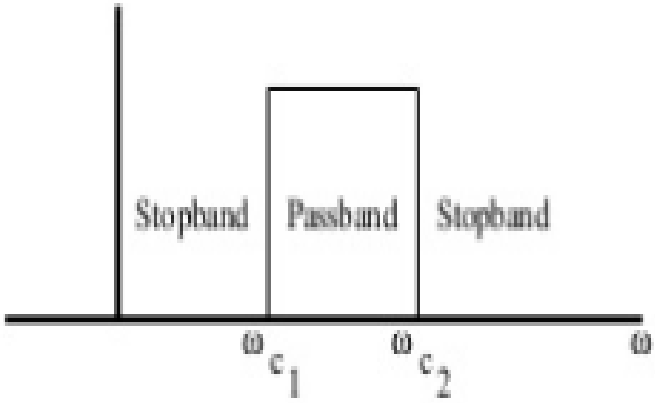
Highpass Filter



Bandstop Filter



Bandpass Filter



Passive Filters

- Made up of passive components - resistors, capacitors and inductors
- No amplifying elements (transistors, op-amps, etc)
- No signal gain
- 1st order - design is simple (just use standard equations to find resonant frequency of the circuit)
- 2nd order - complex equations
- Require no power supplies
- Buffer amplifiers might be required
- Desirable to use inductors with high quality factors

Inductor - BIG PROBLEM!

- Physical size, and large inductance values are required.
- Tuning inductors to the required values is time-consuming and expensive for larger quantities of filters.
- Often prohibitively expensive.
- Difficult to implement at frequencies below 1 kHz.
- Lossy

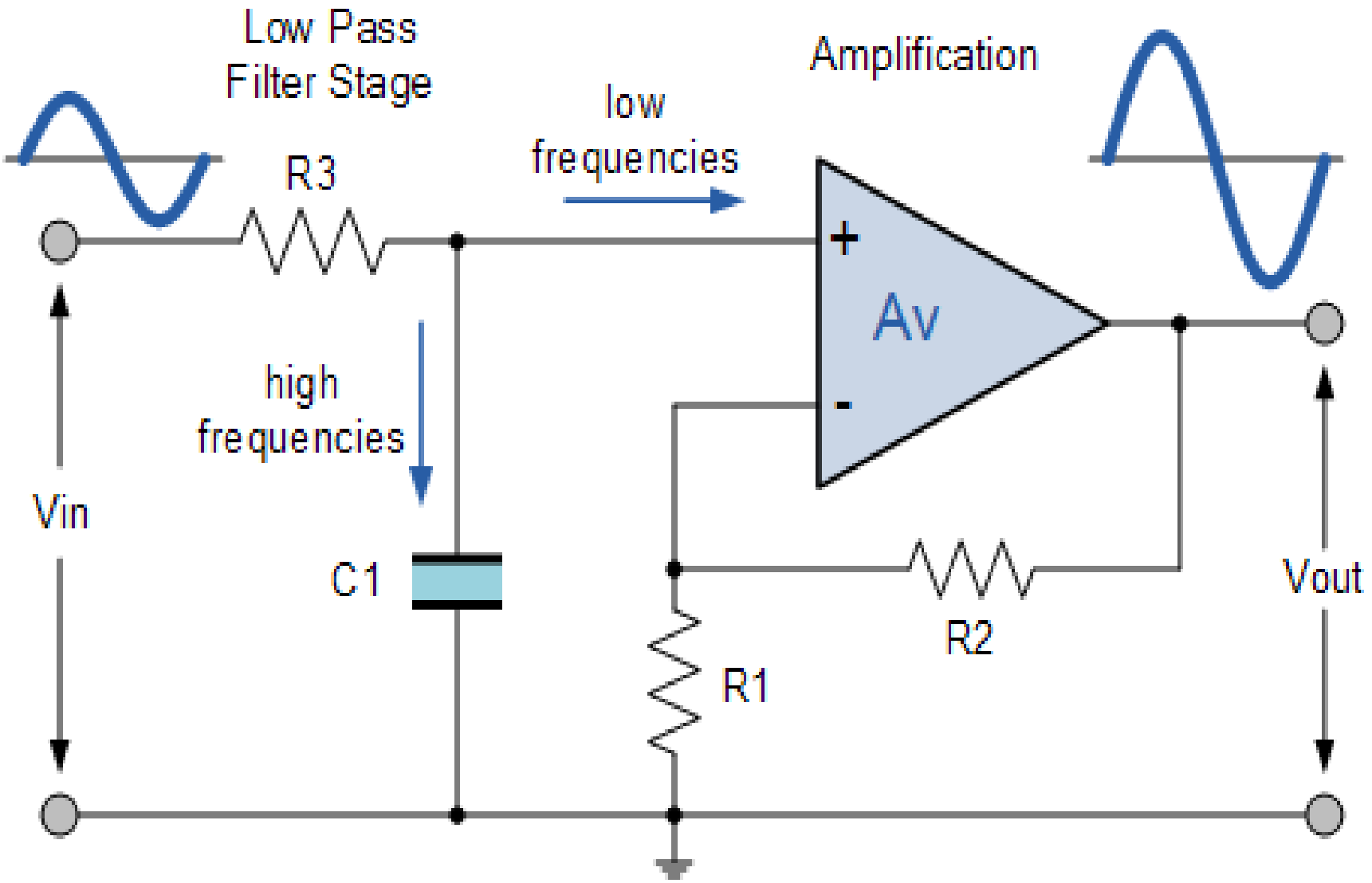
Active Filter

- No inductors
- Made up of op-amps, resistors and capacitors
- Provides arbitrary gain
- Generally easier to design
- High input impedance prevents excessive loading of the driving source
- Low output impedance prevents the filter from being affected by the load
- Easy to adjust over a wide frequency range without altering the desired response

Active Low Pass Filter

- This first-order low pass active filter, consists simply of a passive RC filter stage providing a low frequency path to the input of a non-inverting operational amplifier. If an active filter allows (passes) only **low frequency** components and rejects (blocks) all other high frequency components, then it is called as an **active low pass filter**.

Active Low Pass Filter



Gain of a first-order low pass filter

$$\text{DC gain} = \left(1 + \frac{R_2}{R_1}\right)$$

$$\text{Voltage Gain, } (Av) = \frac{Vout}{Vin} = \frac{A_F}{\sqrt{1 + \left(\frac{f}{fc}\right)^2}}$$

Where:

A_F = the pass band gain of the filter, (1 + R2/R1)

ƒ = the frequency of the input signal in Hertz, (Hz)

ƒc = the cut-off frequency in Hertz, (Hz)

The operation of a low pass active filter can be verified from the frequency gain equation

1. At very low frequencies, ƒ < ƒc $\frac{Vout}{Vin} \cong A_F$
2. At the cut-off frequency, ƒ = ƒc $\frac{Vout}{Vin} = \frac{A_F}{\sqrt{2}} = 0.707\,A_F$
3. At very high frequencies, ƒ > ƒc $\frac{Vout}{Vin} < A_F$

Thus, the **Active Low Pass Filter** has a constant gain A_F from 0Hz to the high frequency cut-off point, f_C. At f_C the gain is $0.707A_F$, and after f_C it decreases at a constant rate as the frequency increases

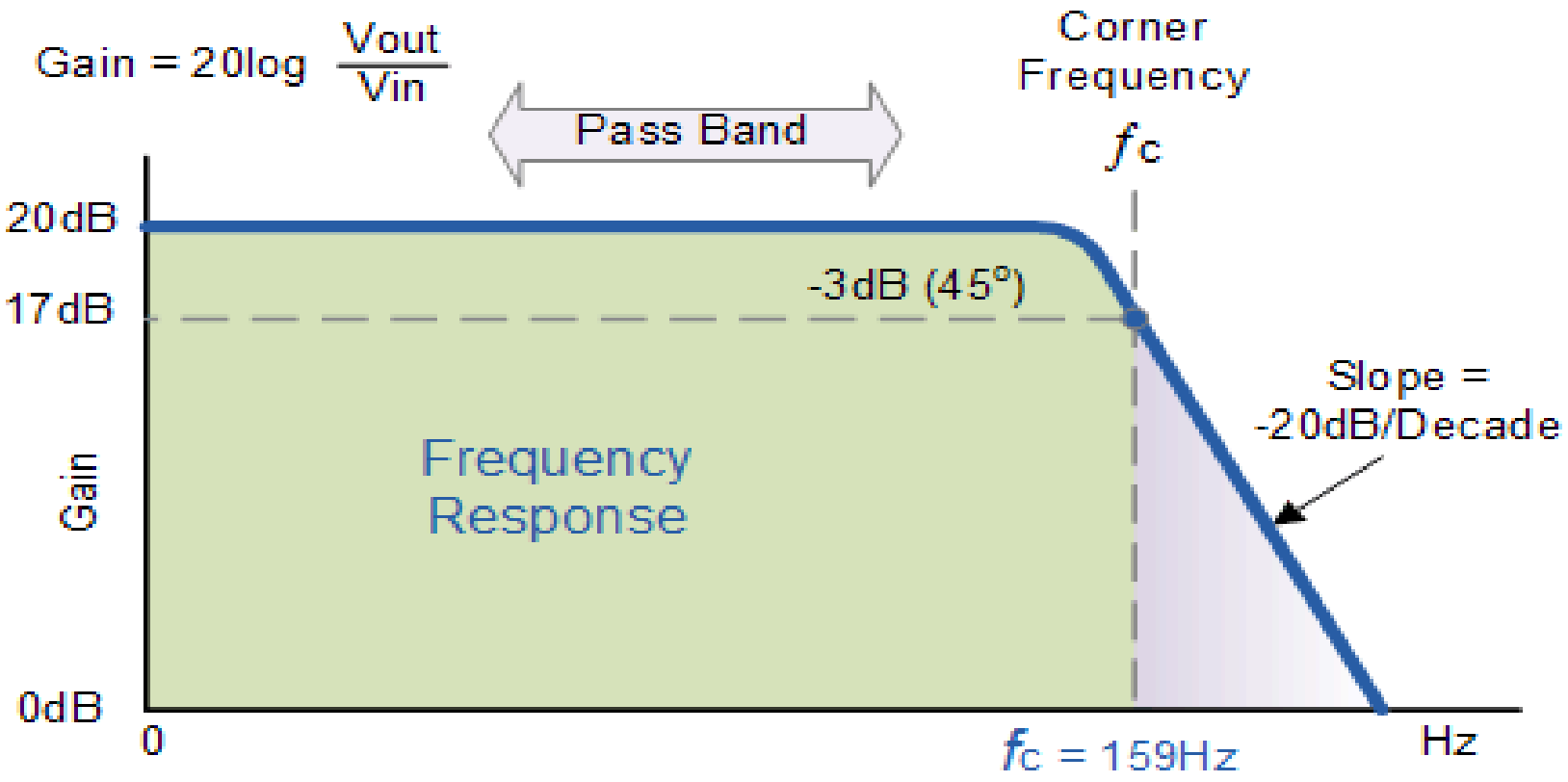
Magnitude of Voltage Gain in (dB)

The gain decreases 20dB (= 20*log(10)) each time the frequency is increased by 10. When dealing with filter circuits the magnitude of the pass band gain of the circuit is generally expressed in *decibels* or *dB* as a function of the voltage gain

$$\mathrm{Av(dB)} = 20\log_{10}\left(\frac{\mathrm{Vout}}{\mathrm{Vin}}\right)$$

$$\therefore \ -3\mathrm{dB} = 20\log_{10}\left(0.707\,\frac{\mathrm{Vout}}{\mathrm{Vin}}\right)$$

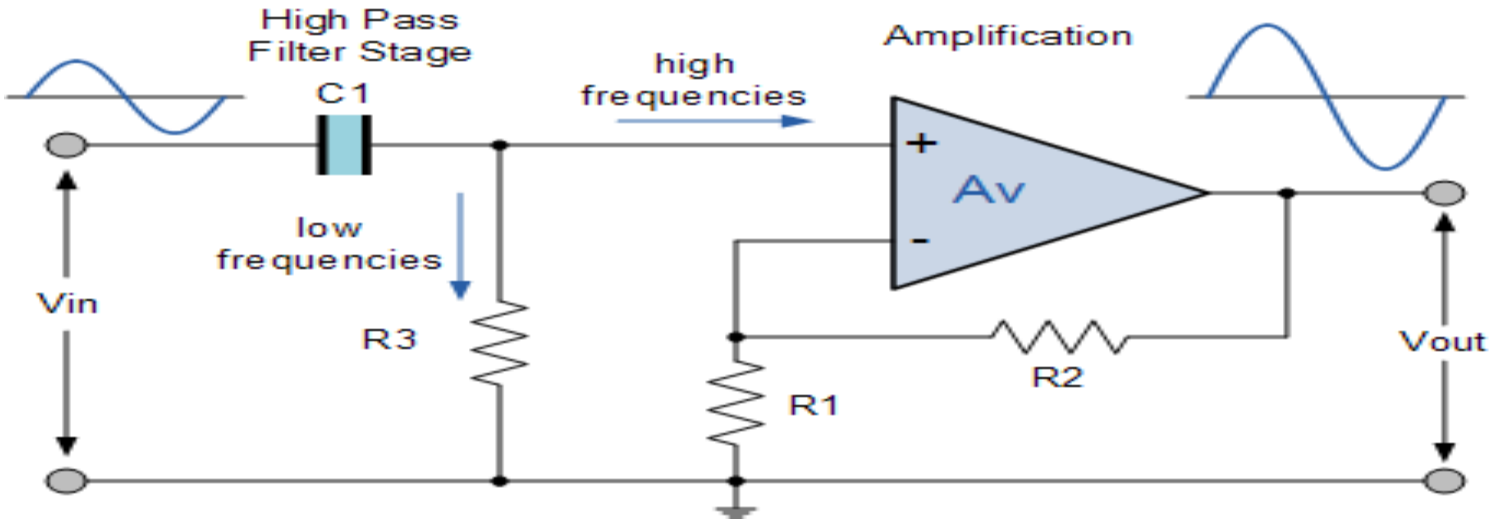
Frequency Response Curve



$$fc = \frac{1}{2\pi RC} Hz$$

Active High Pass Filter

- If an active filter allows (passes) only **high frequency** components and rejects (blocks) all other low frequency components, then it is called an **active high pass filter**.



Gain for an Active High Pass Filter

$$\text{Voltage Gain, (Av)} = \frac{\text{Vout}}{\text{Vin}} = \frac{A_F\left(\frac{f}{fc}\right)}{\sqrt{1+\left(\frac{f}{fc}\right)^2}}$$

Where:

A_F = the Pass band Gain of the filter, (1 + R2/R1)

ƒ = the Frequency of the Input Signal in Hertz, (Hz)

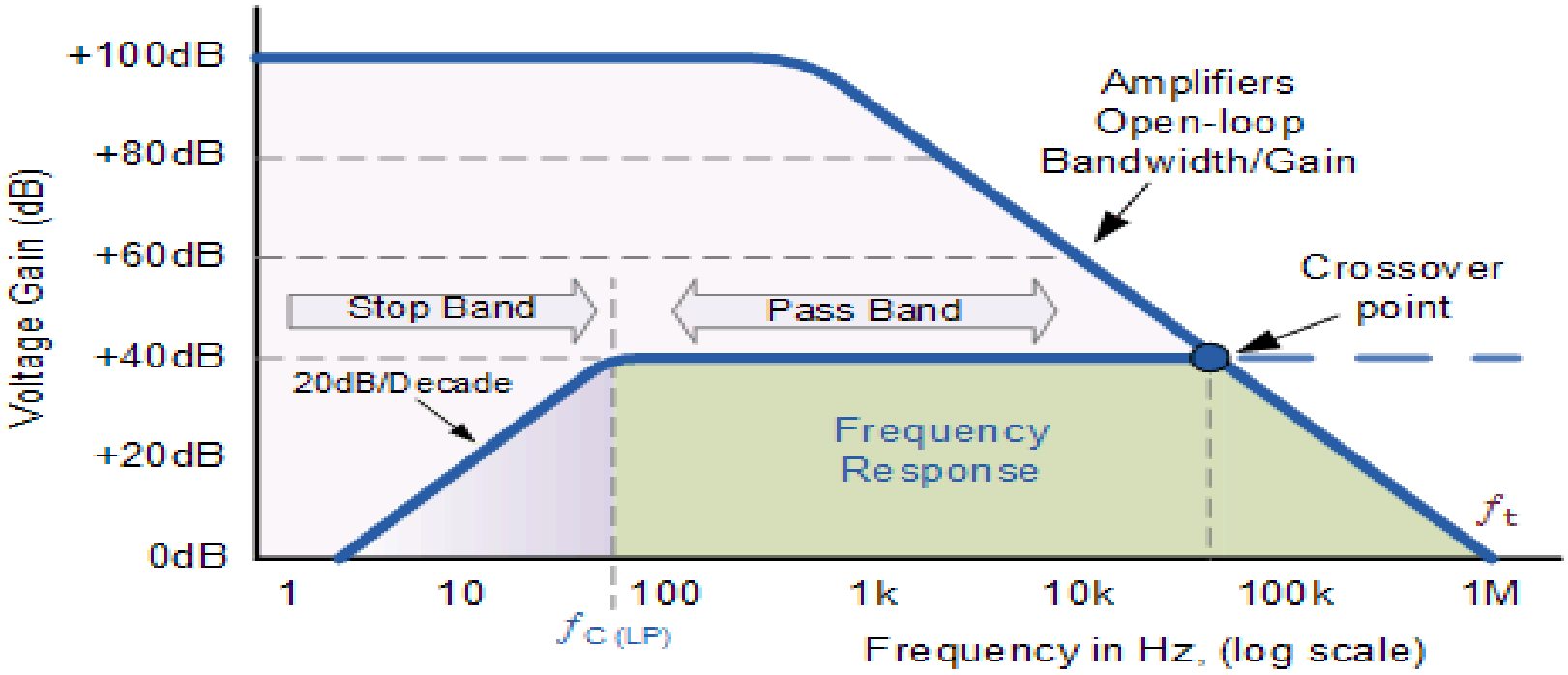
ƒc = the Cut-off Frequency in Hertz, (Hz)

The operation of a high pass active filter can be verified from the frequency gain equation

1. At very low frequencies, ƒ < ƒc $\frac{Vout}{Vin} < A_F$
2. At the cut-off frequency, ƒ = ƒc $\frac{Vout}{Vin} = \frac{A_F}{\sqrt{2}} = 0.707\,A_F$
3. At very high frequencies, ƒ > ƒc $\frac{Vout}{Vin} \cong A_F$

Active High Pass Filter has a gain A_F that increases from 0Hz to the low frequency cut-off point, f_C at 20dB/decade as the frequency increases. At f_C the gain is $0.707*A_F$, and after f_C all frequencies are pass band frequencies so the filter has a constant gain A_F with the highest frequency being determined by the closed loop bandwidth of the op-amp

Frequency Response Curve



$$fc = \frac{1}{2\pi RC}\ Hz$$

Magnitude of Voltage Gain in (dB)

$$\mathrm{Av(dB)} = 20\log_{10}\left(\frac{\mathrm{Vout}}{\mathrm{Vin}}\right)$$

$$\therefore\ -3\mathrm{dB} = 20\log_{10}\left(0.707\,\frac{\mathrm{Vout}}{\mathrm{Vin}}\right)$$

Active Band Pass Filter

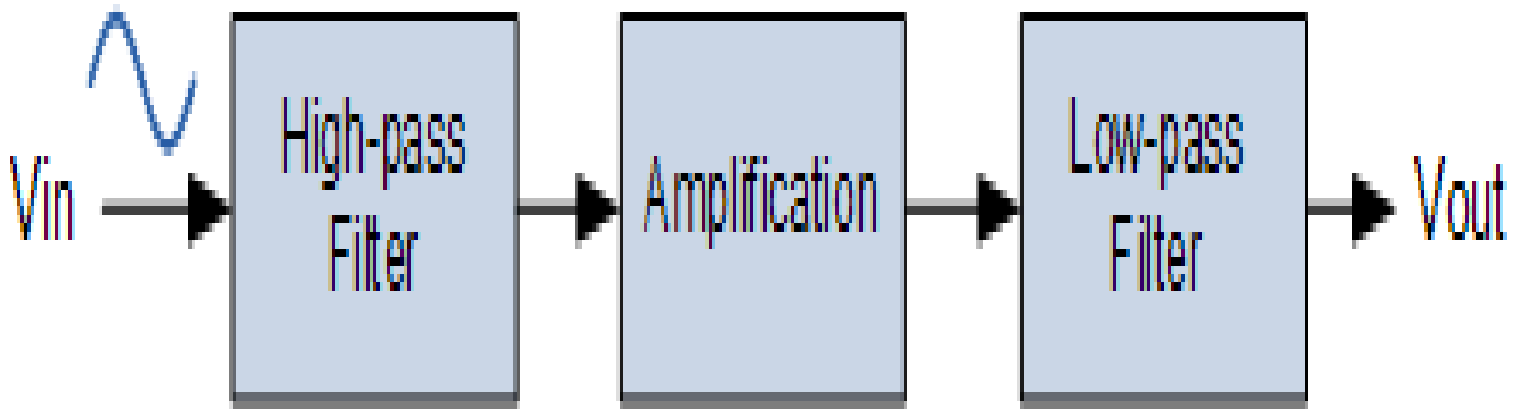
- If an active filter allows (passes) only one band of frequencies, then it is called as an **active band pass filter**. In general, this frequency band lies between low frequency range and high frequency range. So, active band pass filter rejects (blocks) both low and high frequency components.
- The principal characteristic of a **Band Pass Filter** or any filter for that matter, is its ability to pass frequencies relatively unattenuated over a specified band or spread of frequencies called the “Pass Band”.

Active Band Pass Filter

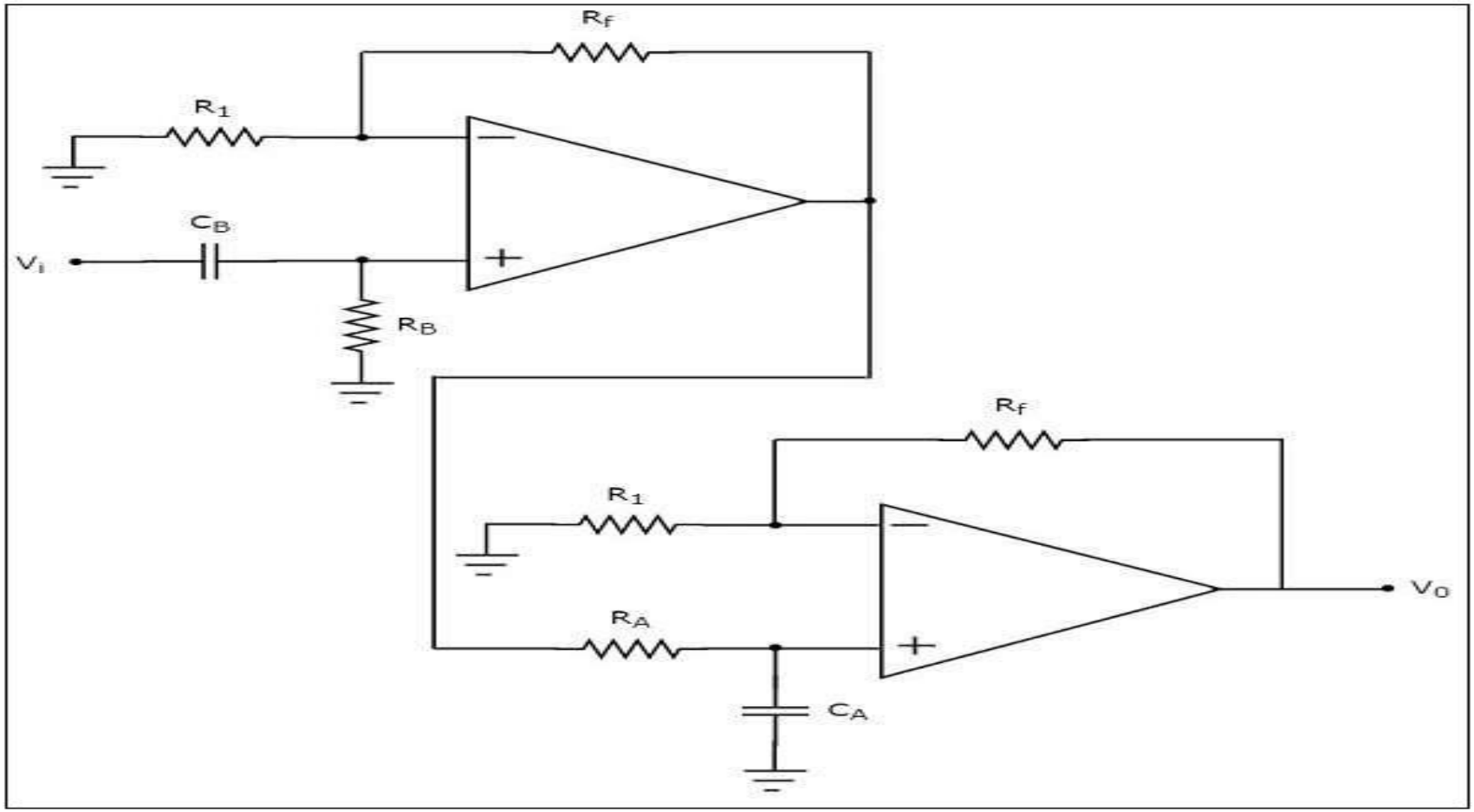
- **Active Band Pass Filter** is slightly different in that it is a frequency selective filter circuit used in electronic systems to separate a signal at one particular frequency, or a range of signals that lie within a certain “band” of frequencies from signals at all other frequencies. This band or range of frequencies is set between two cut-off or corner frequency points labelled the “lower frequency” (f_L) and the “higher frequency” (f_H) while attenuating any signals outside of these two points.

Active Band Pass Filter

- **Active Band Pass Filter** can be easily made by cascading together a single Low Pass Filter with a single High Pass Filter as shown.

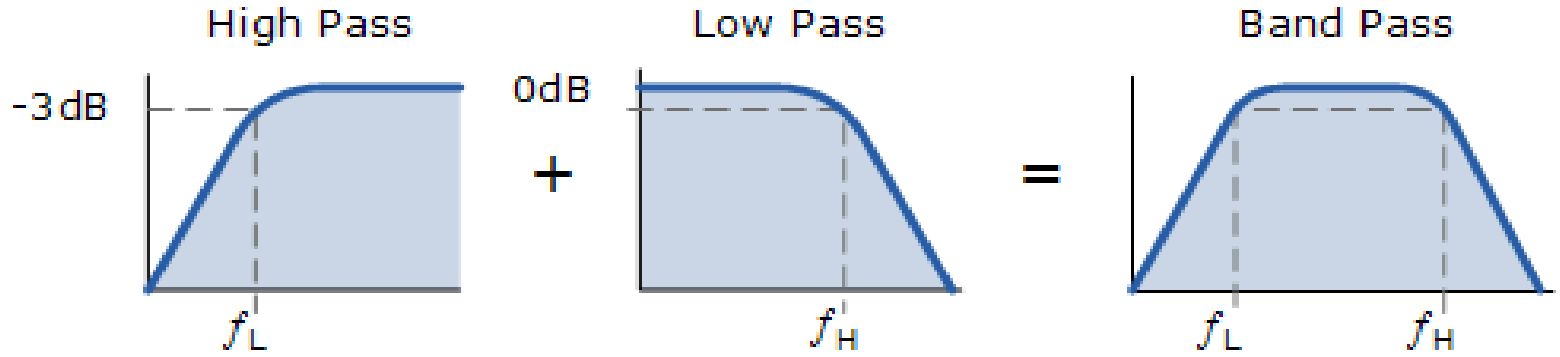


Active Band Pass Filter



Active Band Pass Filter

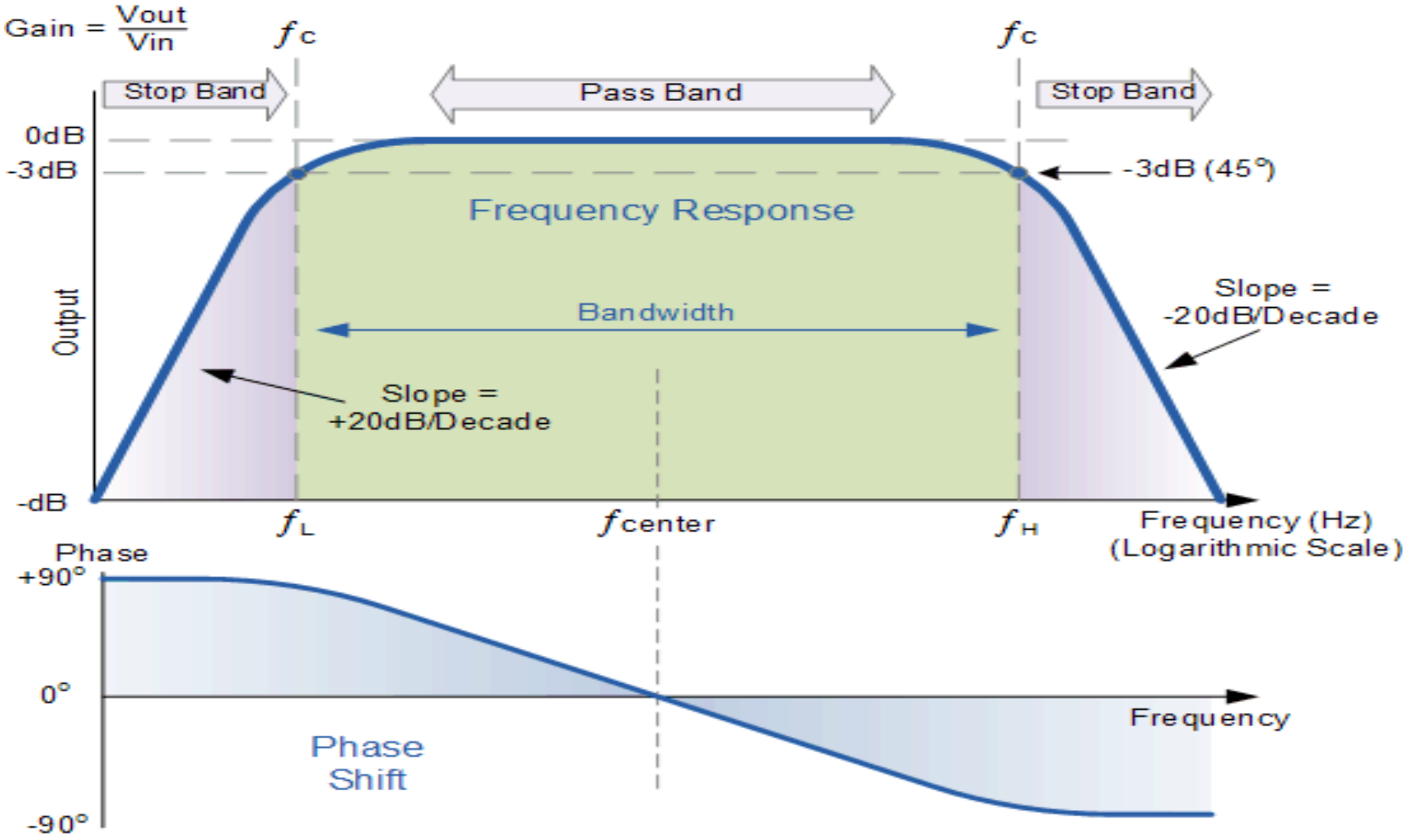
- This cascading together of the individual low and high pass passive filters produces a low “Q-factor” type filter circuit which has a wide pass band. The first stage of the filter will be the high pass stage that uses the capacitor to block any DC biasing from the source. This design has the advantage of producing a relatively flat asymmetrical pass band frequency response with one half representing the low pass response and the other half representing high pass response as shown.



Active Band Pass Filter

- The higher corner point (f_H) as well as the lower corner frequency cut-off point (f_L) are calculated the same as before in the standard first-order low and high pass filter circuits. Obviously, a reasonable separation is required between the two cut-off points to prevent any interaction between the low pass and high pass stages. The amplifier also provides isolation between the two stages and defines the overall voltage gain of the circuit.
- The bandwidth of the filter is therefore the difference between these upper and lower -3dB points. For example, suppose we have a band pass filter whose -3dB cut-off points are set at 200Hz and 600Hz. Then the bandwidth of the filter would be given as: Bandwidth (BW) = 600 – 200 = 400Hz.

Active Band Pass Frequency Response



Resonant Frequency Point

- The actual shape of the frequency response curve for any passive or active band pass filter will depend upon the characteristics of the filter circuit with the curve above being defined as an “ideal” band pass response. An active band pass filter is a **2nd Order** type filter because it has “two” reactive components (two capacitors) within its circuit design.
- As a result of these two reactive components, the filter will have a peak response or **Resonant Frequency** (ƒr) at its “center frequency”, ƒc. The center frequency is generally calculated as being the geometric mean of the two -3dB frequencies between the upper and the lower cut-off points with the resonant frequency (point of oscillation) being given as:

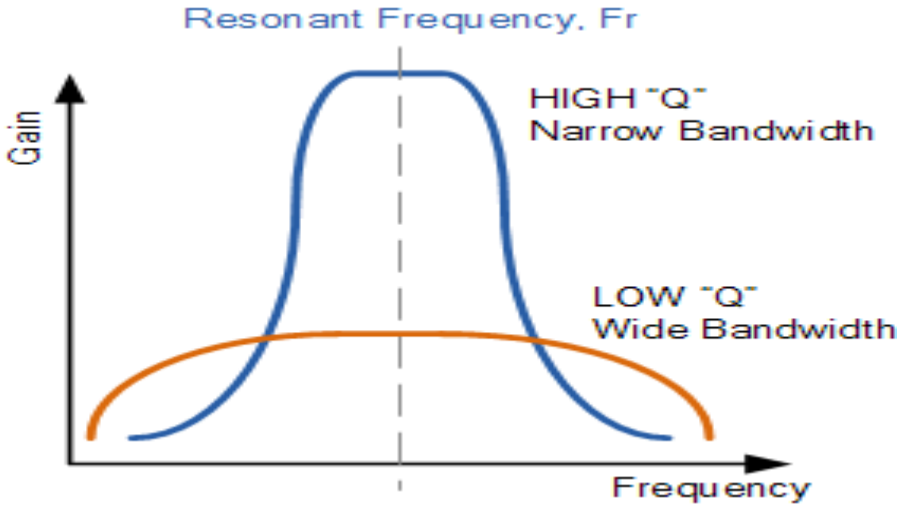
$$fr = \sqrt{f_L \; x \; f_H}$$

Where:
f_r is the resonant or Center Frequency
f_L is the lower -3dB cut-off frequency point
f_H is the upper -3db cut-off frequency point

The “Q” or Quality Factor

- **Band Pass Filter** circuit, the overall width of the actual pass band between the upper and lower -3dB corner points of the filter determines the **Quality Factor** or **Q-point** of the circuit. This **Q Factor** is a measure of how “Selective” or “Un-selective” the band pass filter is towards a given spread of frequencies. The lower the value of the Q factor the wider is the bandwidth of the filter and consequently the higher the Q factor the narrower and more “selective” is the filter.

The “Q” of a band pass filter is the ratio of the **Resonant Frequency**, (ƒr) to the **Bandwidth**, (BW) between the upper and lower -3dB frequencies and is given as:



$$Q = \frac{\text{Resonant Frequency}}{\text{Bandwidth}}$$

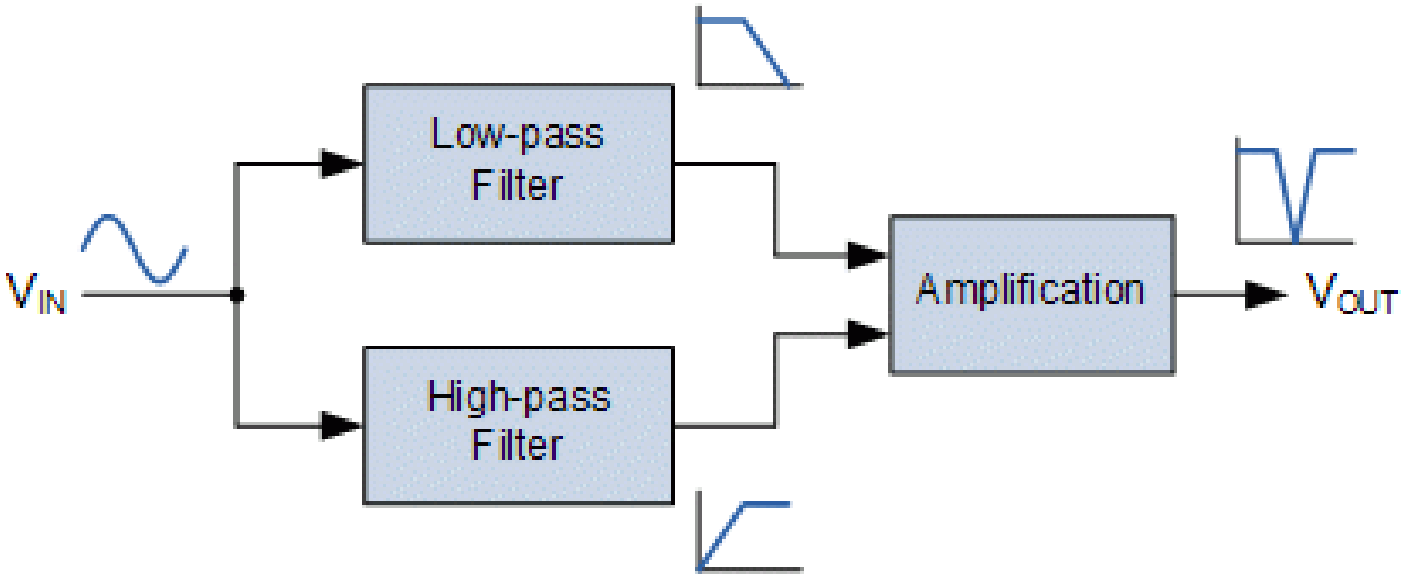
Active Band Stop Filter

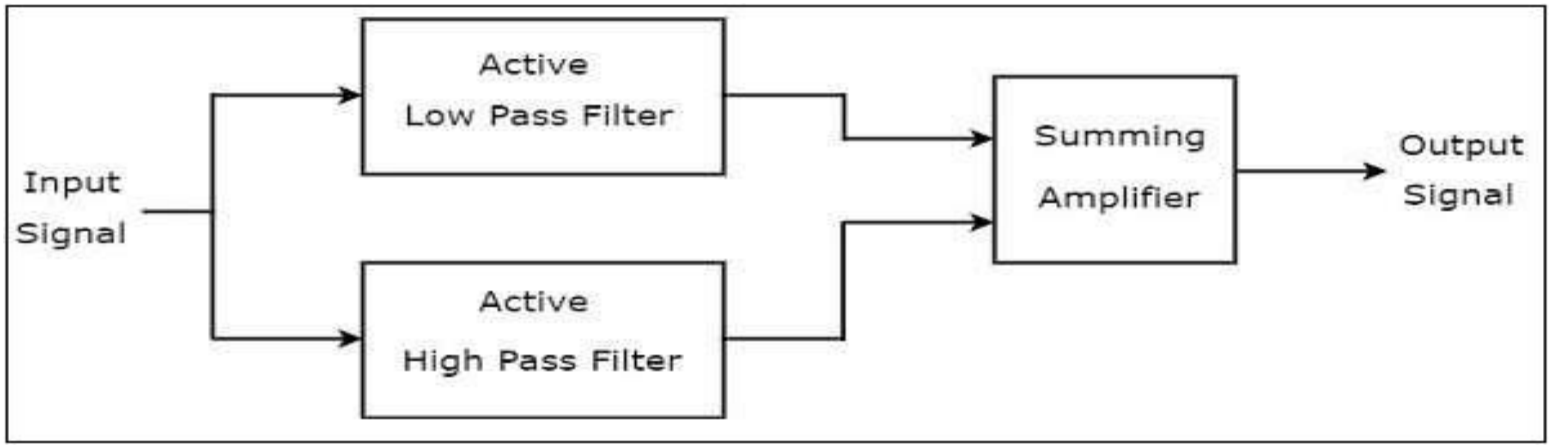
- If an active filter rejects (blocks) a particular band of frequencies, then it is called as an **active band stop filter**. In general, this frequency band lies between low frequency range and high frequency range. So, active band stop filter allows (passes) both low and high frequency components.
- A band Stop Filter known also as a Notch Filter, blocks and rejects frequencies that lie between its two cut-off frequency points passes all those frequencies either side of this range

Active Band Stop Filter

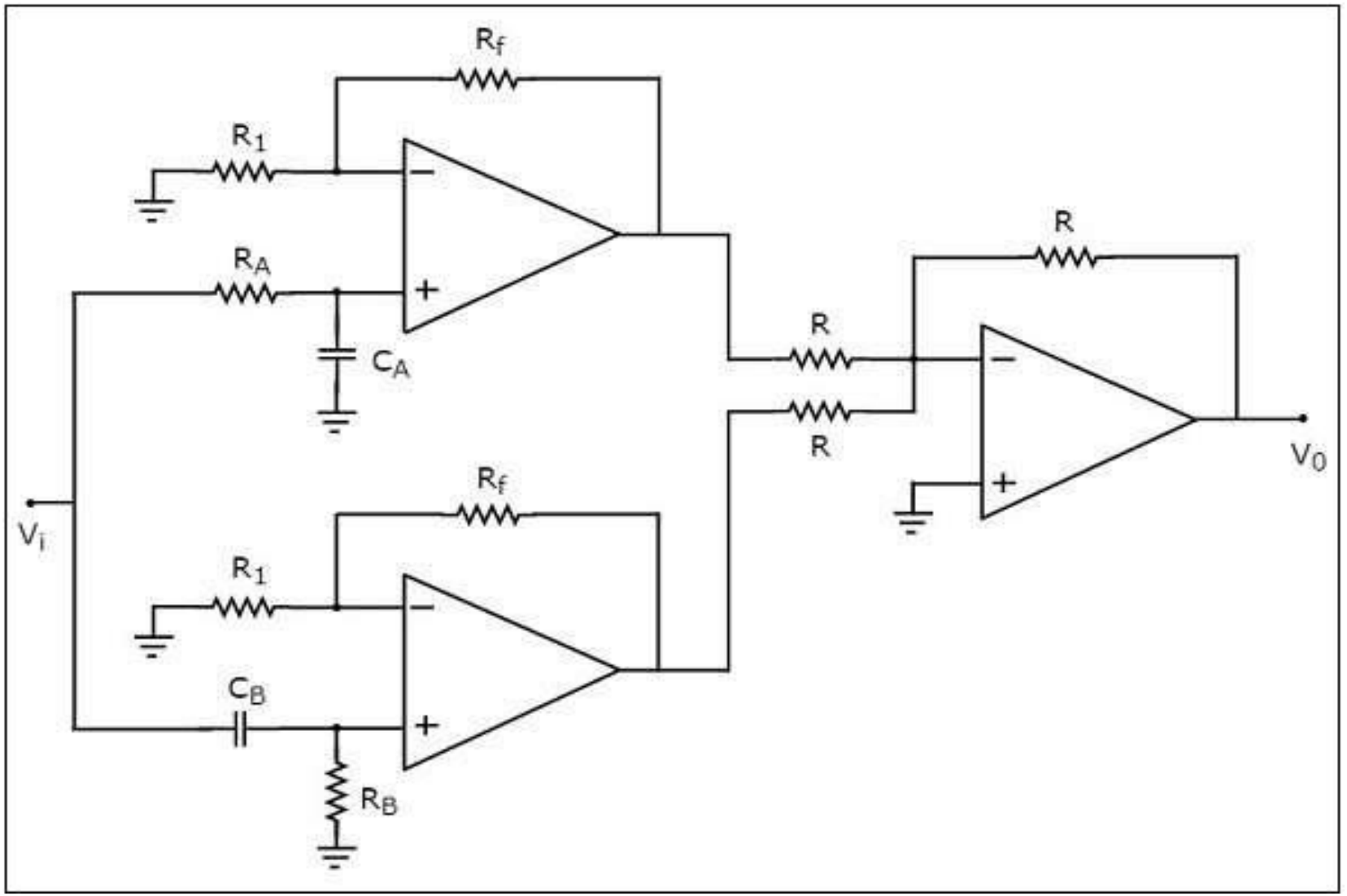
- block diagram of an active band stop filter consists of two blocks in its first stage: an active low pass filter and an active high pass filter. The outputs of these two blocks are applied as inputs to the block that is present in the second stage. So, the **summing amplifier** produces an output, which is the amplified version of sum of the outputs of the active low pass filter and the active high pass filter.
- Therefore, the output of the above block diagram will be the **output of an active band stop** , when we choose the cut-off frequency of low pass filter to be smaller than cut-off frequency of a high pass filter.

Active Band Stop Filter





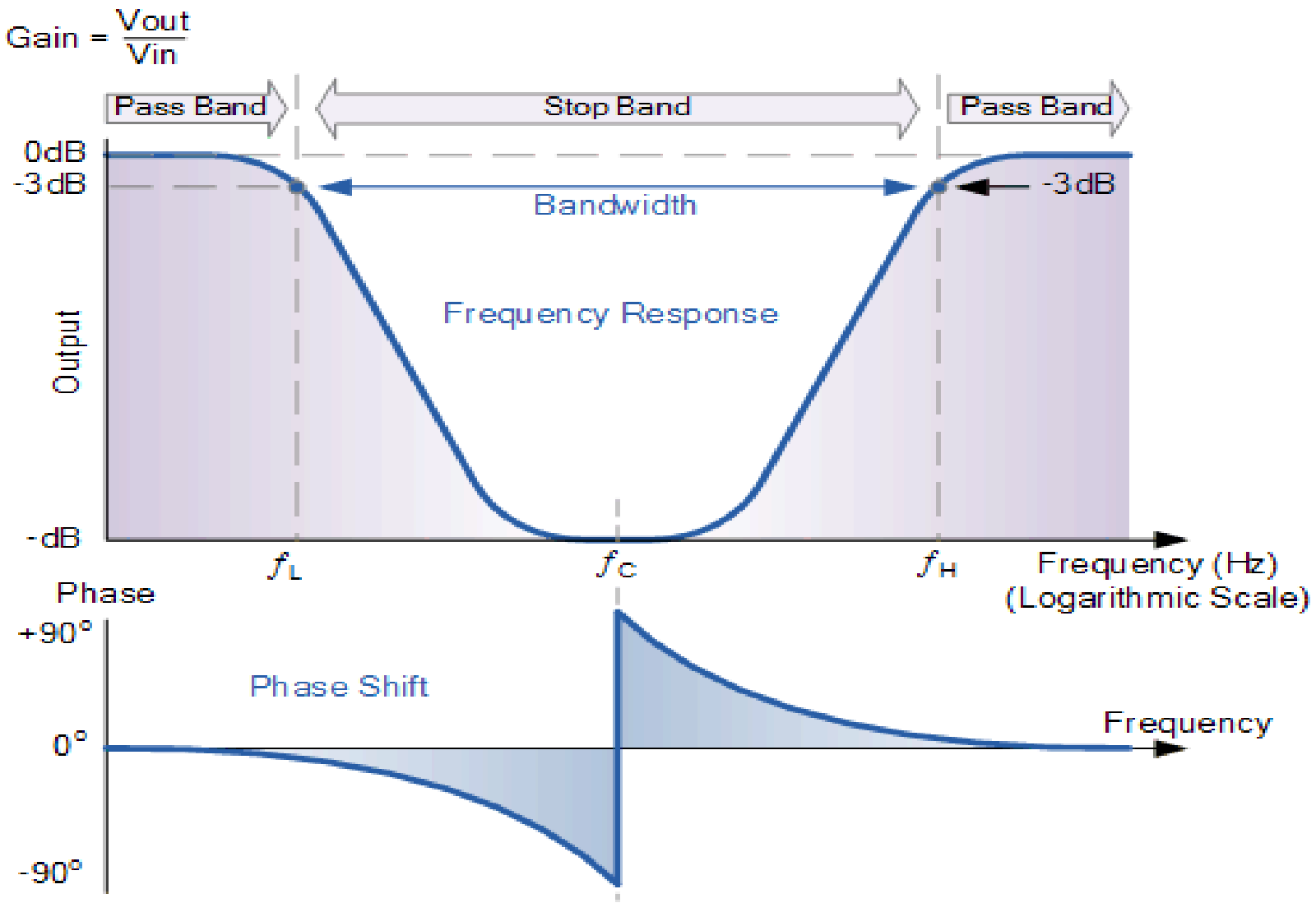
Active Band Stop Filter



Active Band Stop Filter

- Then the function of a band stop filter is too pass all those frequencies from zero (DC) up to its first (lower) cut-off frequency point f_L, and pass all those frequencies above its second (upper) cut-off frequency f_H, but block or reject all those frequencies in-between. Then the filters bandwidth, BW is defined as: $(f_H - f_L)$.

Band Stop Filter Response

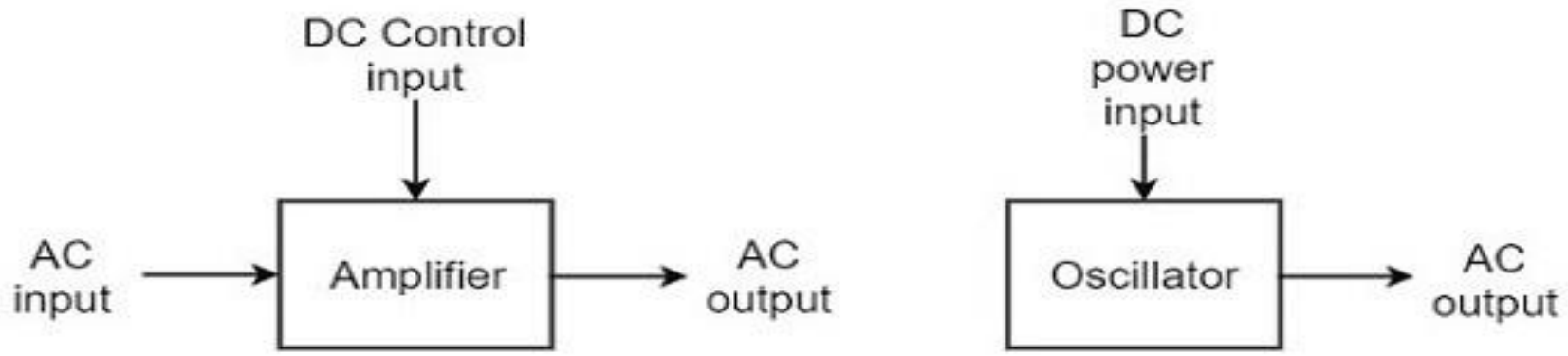


Active Band Stop Filter

- The summing of the high pass and low pass filters means that their frequency responses do not overlap, unlike the band-pass filter. This is due to the fact that their start and ending frequencies are at different frequency points. For example, suppose we have a first-order low-pass filter with a cut-off frequency, f_L of 200Hz connected in parallel with a first-order high-pass filter with a cut-off frequency, f_H of 800Hz. As the two filters are effectively connected in parallel, the input signal is applied to both filters simultaneously as shown above.
- All of the input frequencies below 200Hz would be passed unattenuated to the output by the low-pass filter. Likewise, all input frequencies above 800Hz would be passed unattenuated to the output by the high-pass filter. However, and input signal frequencies in-between these two frequency cut-off points of 200Hz and 800Hz, that is f_L to f_H would be rejected by either filter forming a notch in the filters output response.
- In other words a signal with a frequency of 200Hz or less and 800Hz and above would pass unaffected but a signal frequency of say 500Hz would be rejected as it is too high to be passed by the low-pass filter and too low to be passed by the high-pass filter.

Sinusoidal Oscillators

- An **oscillator** generates output without any ac input signal. An electronic oscillator is a circuit which converts dc energy into ac at a very high frequency. An amplifier with a positive feedback can be understood as an oscillator.



Amplifier vs. Oscillator

- An **amplifier** increases the signal strength of the input signal applied, whereas an **oscillator** generates a signal without that input signal, but it requires dc for its operation. This is the main difference between an amplifier and an oscillator.
- Take a look at the following illustration. It clearly shows how an amplifier takes energy from d.c. power source and converts it into a.c. energy at signal frequency. An oscillator produces an oscillating a.c. signal on its own.
- The frequency, waveform, and magnitude of a.c. power generated by an amplifier, is controlled by the a.c. signal voltage applied at the input, whereas those for an oscillator are controlled by the components in the circuit itself, which means no external controlling voltage is required.

Classification of Oscillators

- Electronic oscillators are classified mainly into the following two categories −
- **Sinusoidal Oscillators** − The oscillators that produce an output having a sine waveform are called **sinusoidal** or **harmonic oscillators**. Such oscillators can provide output at frequencies ranging from 20 Hz to 1 GHz.
- **Non-sinusoidal Oscillators** − The oscillators that produce an output having a square, rectangular or saw-tooth waveform are called **non-sinusoidal** or **relaxation oscillators**. Such oscillators can provide output at frequencies ranging from 0 Hz to 20 MHz.

Sinusoidal Oscillators

- Sinusoidal oscillators can be classified in the following categories −
- **Tuned Circuit Oscillators** − These oscillators use a tuned-circuit consisting of inductors (L) and capacitors (C) and are used to generate high-frequency signals. Thus they are also known as radio frequency R.F. oscillators. Such oscillators are Hartley, Colpitts, Clapp-oscillators etc.
- **RC Oscillators** − There oscillators use resistors and capacitors and are used to generate low or audio-frequency signals. Thus they are also known as audio-frequency (A.F.) oscillators. Such oscillators are Phase –shift and Wein-bridge oscillators.
- **Crystal Oscillators** − These oscillators use quartz crystals and are used to generate highly stabilized output signal with frequencies up to 10 MHz. The Piezo oscillator is an example of a crystal oscillator.
- **Negative-resistance Oscillator** − These oscillators use negative-resistance characteristic of the devices such as tunnel devices. A tuned diode oscillator is an example of a negative-resistance oscillator.

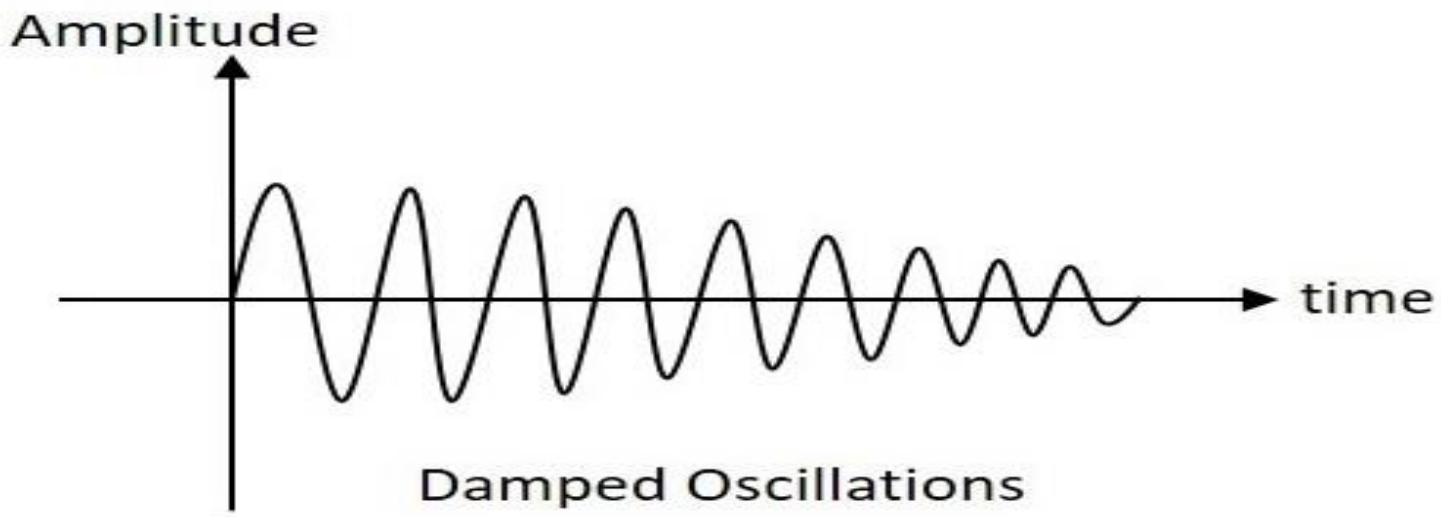
Nature of Sinusoidal Oscillations

- The nature of oscillations in a sinusoidal wave are generally of two types. They are **damped** and **undamped oscillations**.

Damped Oscillations

- The electrical oscillations whose amplitude goes on decreasing with time are called as **Damped Oscillations**. The frequency of the damped oscillations may remain constant depending upon the circuit parameters.

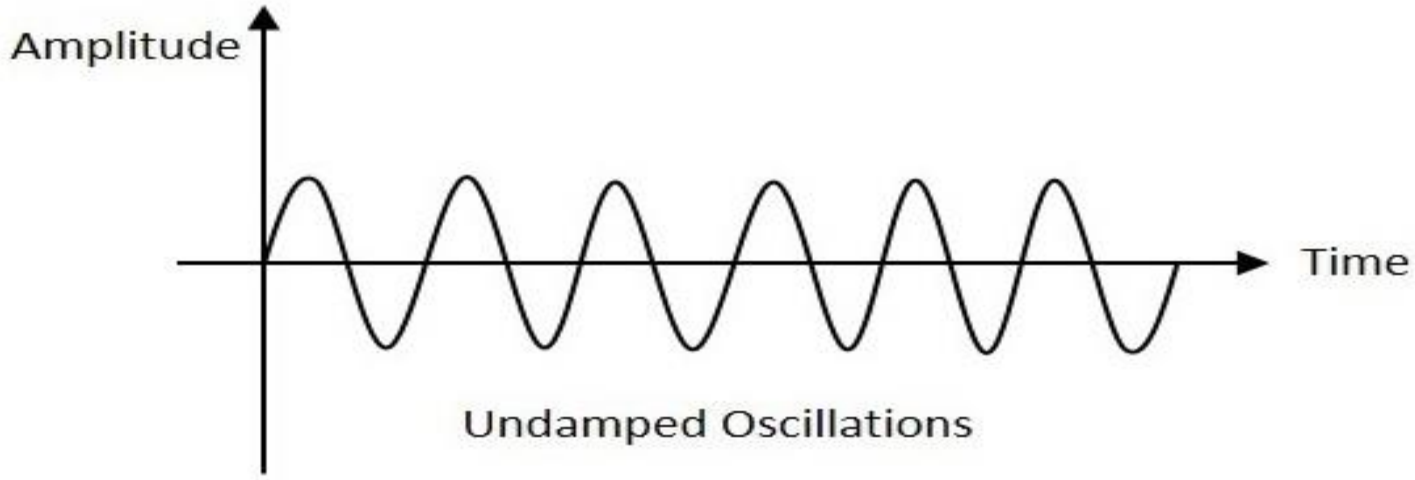
  Damped oscillations are generally produced by the oscillatory circuits that produce power losses and doesn't compensate if required.



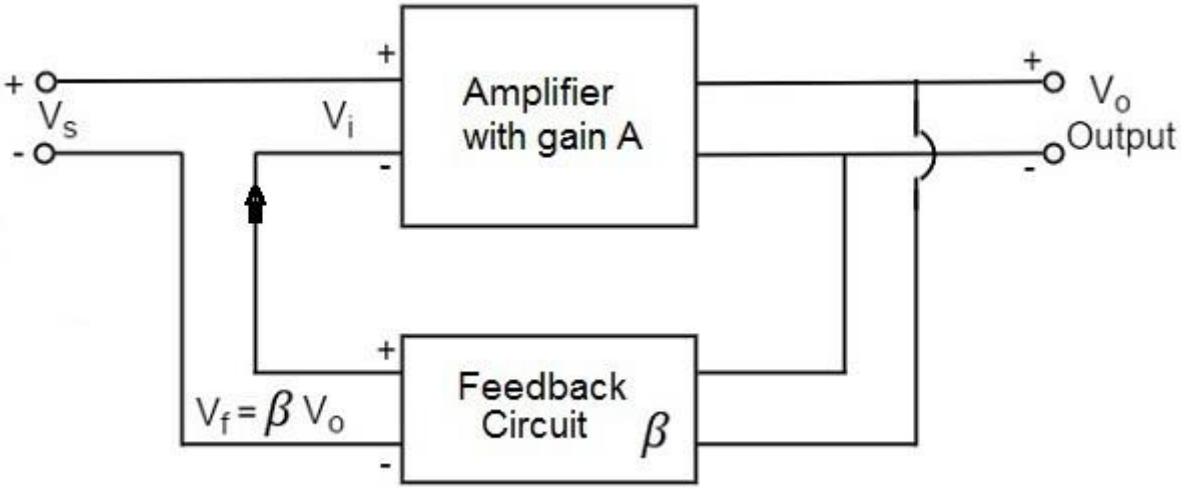
Undamped Oscillations

- The electrical oscillations whose amplitude remains constant with time are called as **Undamped Oscillations**. The frequency of the Undamped oscillations remains constant.

  Undamped oscillations are generally produced by the oscillatory circuits that produce no power losses and follow compensation techniques if any power losses occur.



The Barkhausen Criterion



The block diagram of a sinusoidal oscillator shown above produces sinusoidal oscillations, when the following **two conditions** are satisfied −

•The **loop gain** Avβ of the above block diagram of sinusoidal oscillator must be greater than or equal to **unity**. Here, Av and β are the gain of amplifier and gain of the feedback network, respectively.

•The total **phase shift** around the loop of the above block diagram of a sinusoidal oscillator must be either $\mathbf{0^0}$ or $\mathbf{360^0}$.

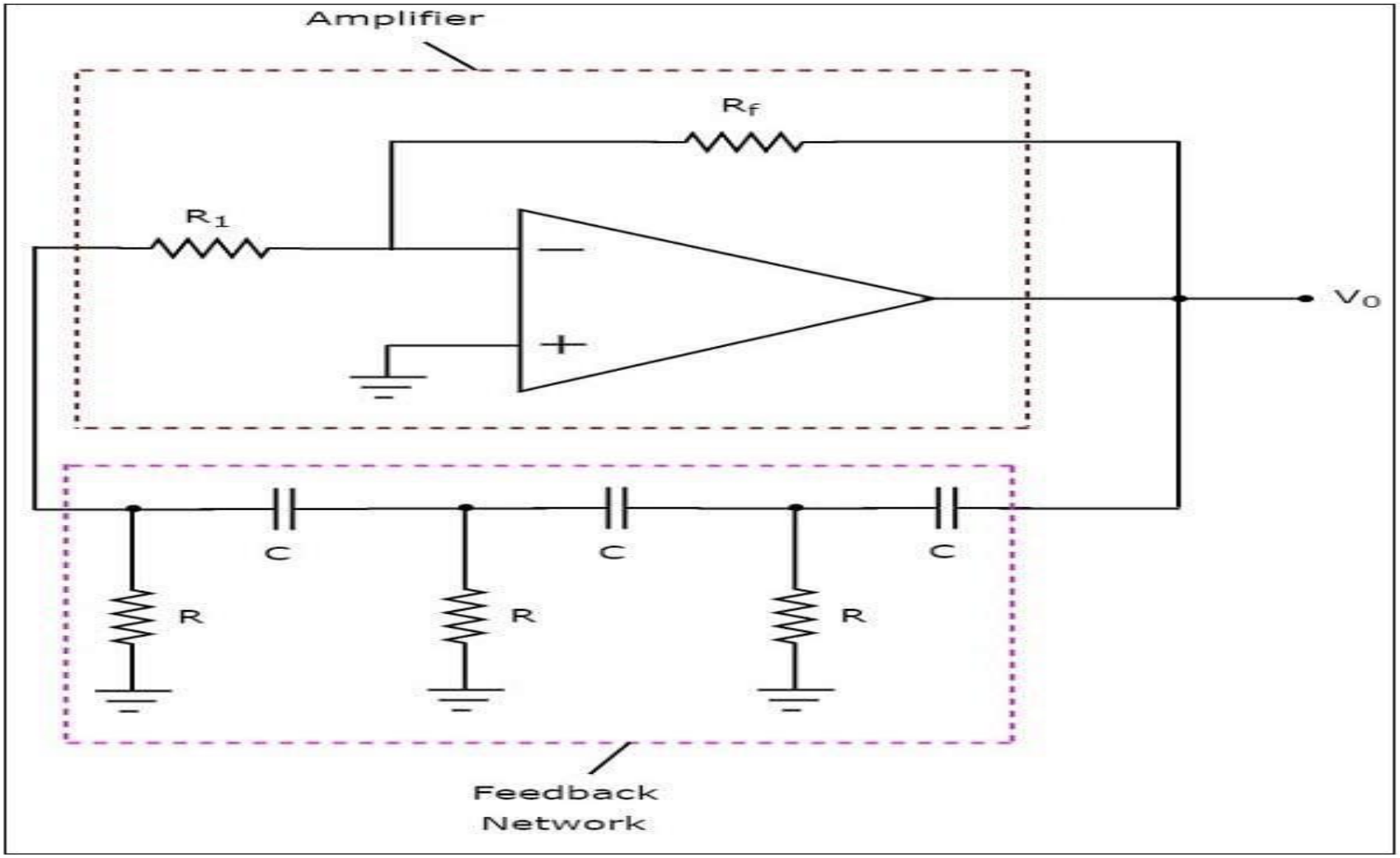
$$\mathbf{A\beta = 1,\ A_f = \infty.}$$

The above two conditions together are called as **Barkhausen criteria**.

RC phase shift oscillator

- The op-amp based oscillator, which produces a sinusoidal voltage signal at the output with the help of an inverting amplifier and a feedback network is known as a **RC phase shift oscillator**. This feedback network consists of three cascaded RC sections.

RC phase shift oscillator



RC phase shift oscillator

- In the above circuit, the op-amp is operating in **inverting mode**. Hence, it provides a phase shift of 180^0. The feedback network present in the above circuit also provides a phase shift of 180^0, since each RC section provides a phase shift of 60^0. Therefore, the above circuit provides a total phase shift of 360^0 at some frequency.

RC phase shift oscillator

- The **output frequency** of a RC phase shift oscillator is –

$$f = \frac{1}{2\Pi RC\sqrt{6}}$$

- The **gain** A_v of an inverting amplifier should be greater than or equal to -29,

$$i.e., -\frac{R_f}{R_1} \geq -29$$

$$=> \frac{R_f}{R_1} \geq -29$$

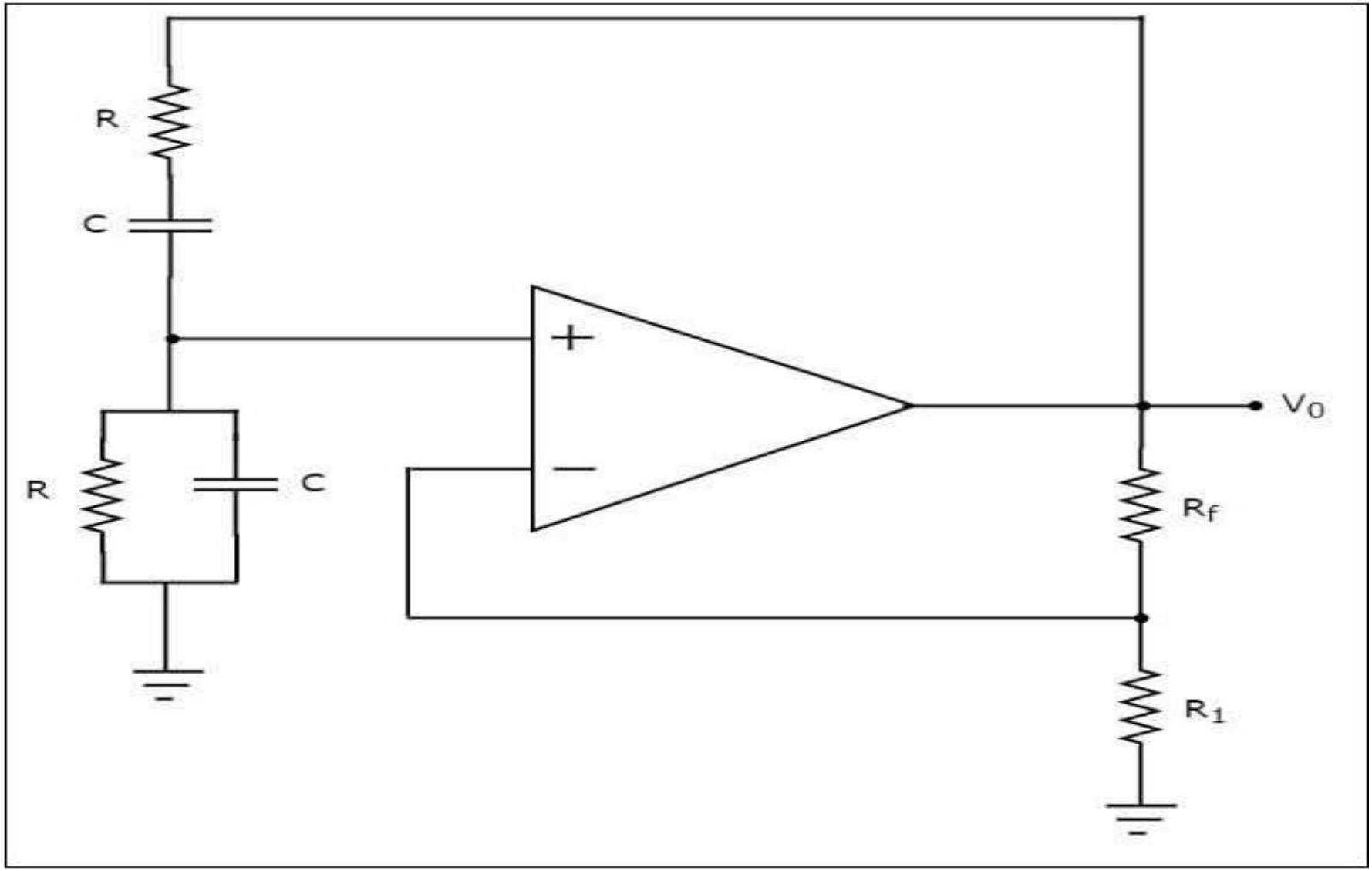
$$=> R_f \geq 29R_1$$

So, we should consider the value of feedback resistor R_f , as minimum of 29 times the value of resistor R_1 , in order to produce sustained oscillations at the output of a RC phase shift oscillator.

Wien Bridge Oscillator

- The op-amp based oscillator, which produces a sinusoidal voltage signal at the output with the help of a non-inverting amplifier and a feedback network is known as **Wien bridge oscillator**.

Wien Bridge Oscillator



Wien Bridge Oscillator

- In the circuit shown above for Wein bridge oscillator, the op-amp is operating in **non inverting mode**. Hence, it provides a phase shift of 00. So, the feedback network present in the above circuit should not provide any phase shift.
- If the feedback network provides some phase shift, then we have to **balance the bridge** in such a way that there should not be any phase shift. So, the above circuit provides a total phase shift of 0^0 at some frequency.

Wien Bridge Oscillator

- The **output frequency** of Wien bridge oscillator is

$$f = \frac{1}{2\Pi RC}$$

- The **gain** A_v of the non-inverting amplifier should be greater than or equal to 3

$$i.e., 1 + \frac{R_f}{R_1} \geq 3$$

$$=> \frac{R_f}{R_1} \geq 2$$

$$=> R_f \geq 2R_1$$

So, we should consider the value of feedback resistor R_f at least twice the value of resistor, R_1 in order to produce sustained oscillations at the output of Wien bridge oscillator.

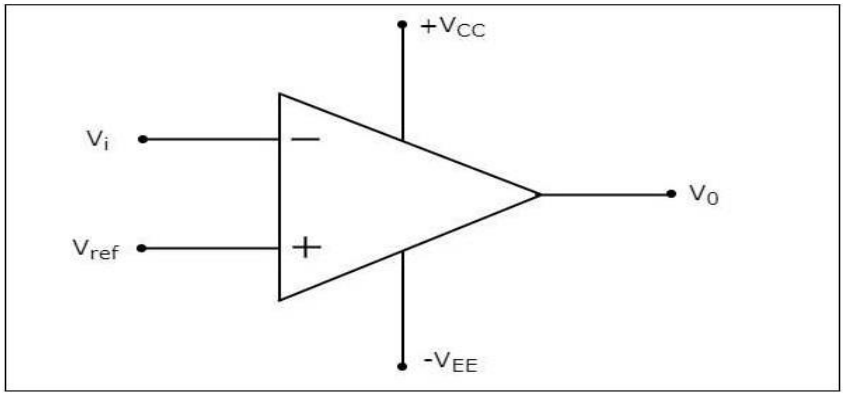
Comparators

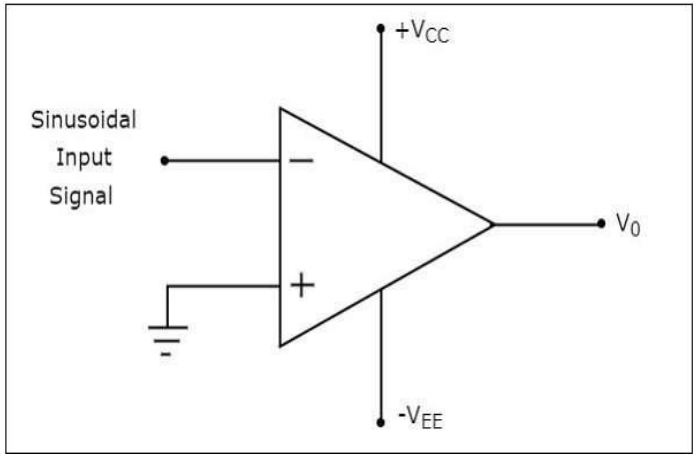
- A **comparator** is an electronic circuit, which compares the two inputs that are applied to it and produces an output. The output value of the comparator indicates which of the inputs is greater or lesser.
- comparator falls under non-linear applications of ICs.

Inverting Comparator

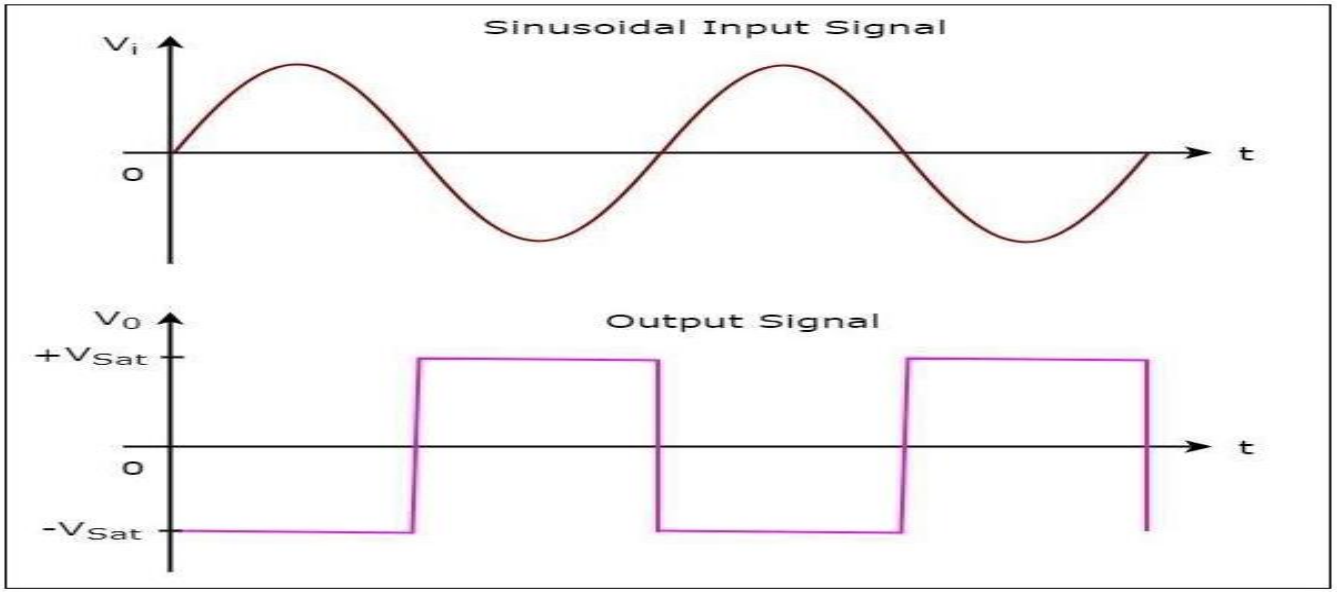
- An **inverting comparator** is an op-amp based comparator for which a reference voltage is applied to its non-inverting terminal and the input voltage is applied to its inverting terminal. This comparator is called as **inverting** comparator because the input voltage, which has to be compared is applied to the inverting terminal of op-amp.

- The **operation** of an inverting comparator is very simple. It produces one of the two values, +Vsat and −Vsat at the output based on the values of its input voltage Vi and the reference voltage Vref.
- The output value of an inverting comparator will be −Vsat, for which the input Vi voltage is greater than the reference voltage Vref.
- The output value of an inverting comparator will be +Vsat, for which the input Vi is less than the reference voltage Vref.





- During the **positive half cycle** of the sinusoidal input signal, the voltage present at the inverting terminal of op-amp is greater than zero volts. Hence, the output value of the inverting comparator will be equal to −Vsat during positive half cycle of the sinusoidal input signal.
- Similarly, during the **negative half cycle** of the sinusoidal input signal, the voltage present at the inverting terminal of the op-amp is less than zero volts. Hence, the output value of the inverting comparator will be equal to +Vsat during negative half cycle of the sinusoidal input signal.



- In the figure shown above, we can observe that the output transitions either from −Vsat to +Vsat or from +Vsat to −Vsat whenever the sinusoidal input signal is crossing zero volts. In other words, output changes its value when the input is crossing zero volts. Hence, the above circuit is also called as **inverting zero crossing detector.**

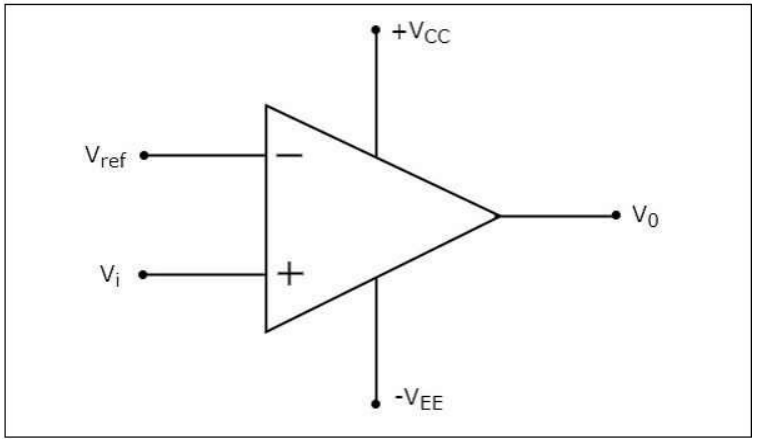
Non-Inverting Comparator

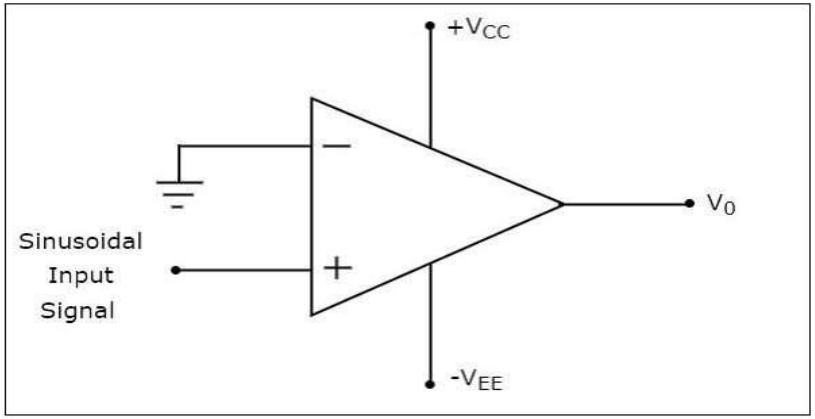
- A non-inverting comparator is an op-amp based comparator for which a reference voltage is applied to its inverting terminal and the input voltage is applied to its non-inverting terminal. This op-amp based comparator is called as **non-inverting** comparator because the input voltage, which has to be compared is applied to the non-inverting terminal of the op-amp.

The **operation** of a non-inverting comparator is very simple. It produces one of the two values, +Vsat and −Vsat at the output based on the values of input voltage Vt and the reference voltage +Vref.

•The output value of a non-inverting comparator will be +Vsat, for which the input voltage Vi is greater than the reference voltage +Vref.

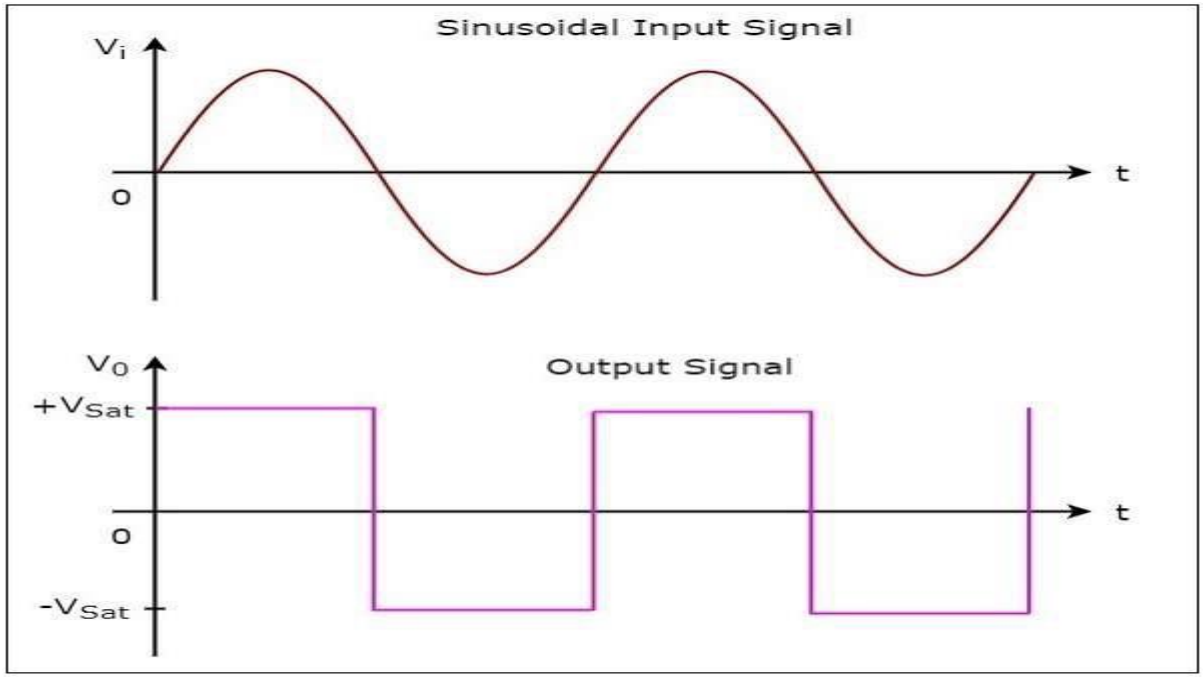
•The output value of a non-inverting comparator will be −Vsat, for which the input voltage Vi is less than the reference voltage ++Vref.





•During the **positive half cycle** of the sinusoidal input signal, the voltage present at the non-inverting terminal of op-amp is greater than zero volts. Hence, the output value of a non-inverting comparator will be equal to +Vsat during the positive half cycle of the sinusoidal input signal.

•Similarly, during the **negative half cycle** of the sinusoidal input signal, the voltage present at the non-inverting terminal of op-amp is less than zero volts. Hence, the output value of non-inverting comparator will be equal to −Vsat during the negative half cycle of the sinusoidal input signal.



Non-Inverting Comparator

- From the figure shown above, we can observe that the output transitions either
  from +Vsat to −Vsat or
  from −Vsat to +Vsat whenever the sinusoidal input signal crosses zero volts. That means, the output changes its value when the input is crossing zero volts. Hence, the above circuit is also called as **non-inverting zero crossing detector**.

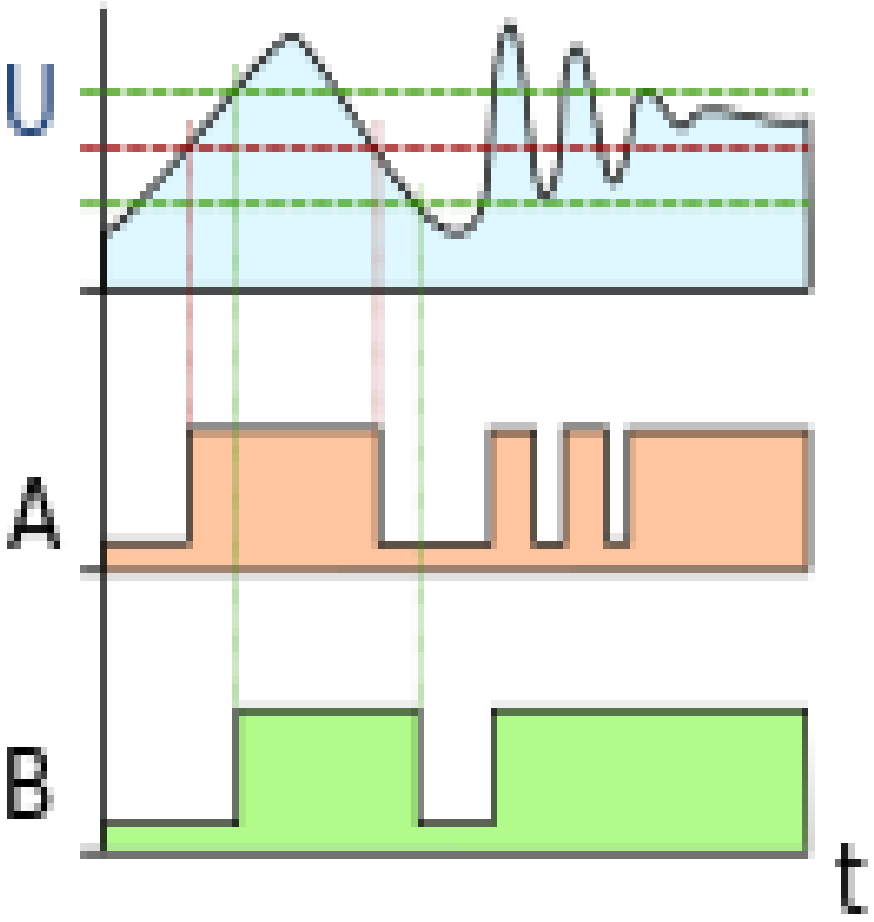
Schmitt trigger

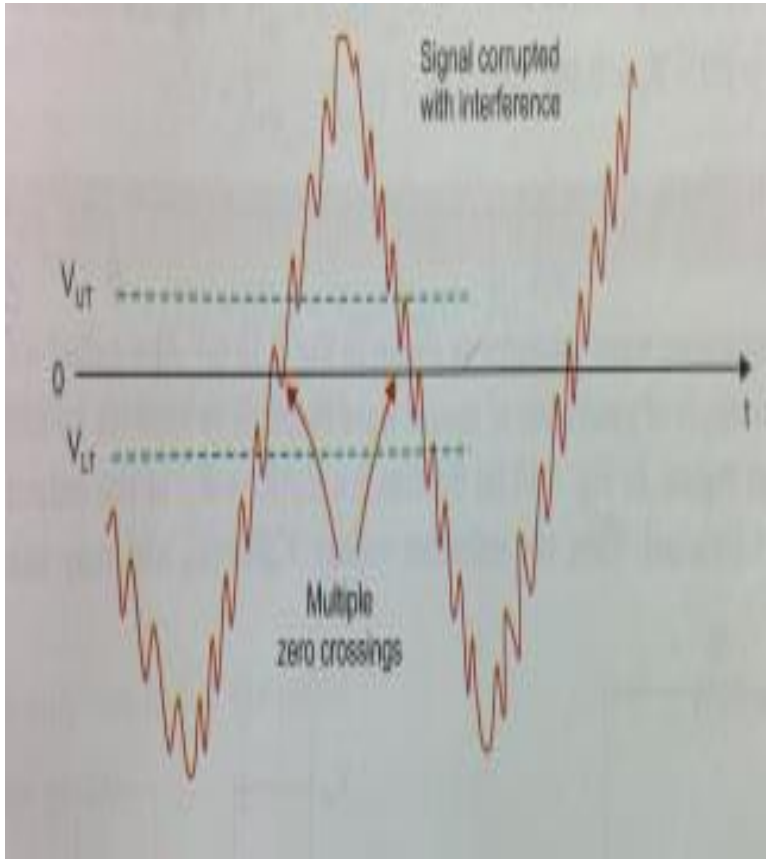
- Schmitt trigger is a comparator circuit with positive feedback ,as gain can be increased greatly.
- The major application of this comparator is to overcome the noise voltages which reduced the problem with zero crossing detector circuit.
- It converts the analog signal to digital signal.

Schmitt trigger

- consider a clean signal and with noise signal crossing zero axis a number of times then the normal zero crossing detector will not deliver the same output even though both signals are same but of course the noise is included in other signal .But the trigger circuit reject the interference with zero crossings and takes the crossings of Vut and VLt only .

Schmitt trigger

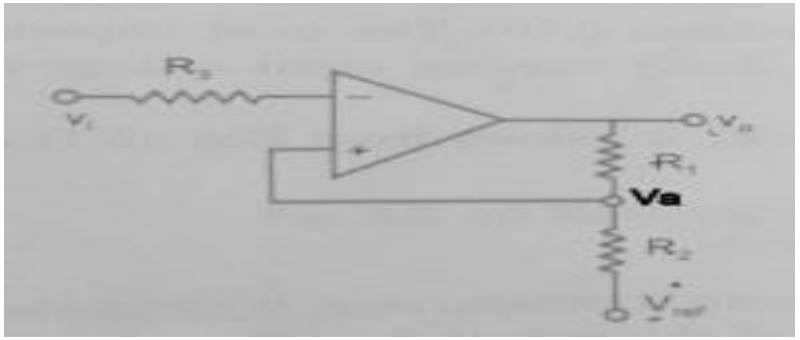




Schmitt trigger

- Vref =Reference voltage
- Vo=Output voltage
- The input voltage Vi triggers the output Vo every time it exceeds certain voltage levels .These voltage levels are called upper threshold voltage and lower threshold voltage.

$$V_a = V_{ref}\frac{R1}{R1+R2} + V_o\frac{R2}{R1+R2}$$



Schmitt trigger

- Va =VUT
- (upper threshold voltage) for Vo=+Vsat then

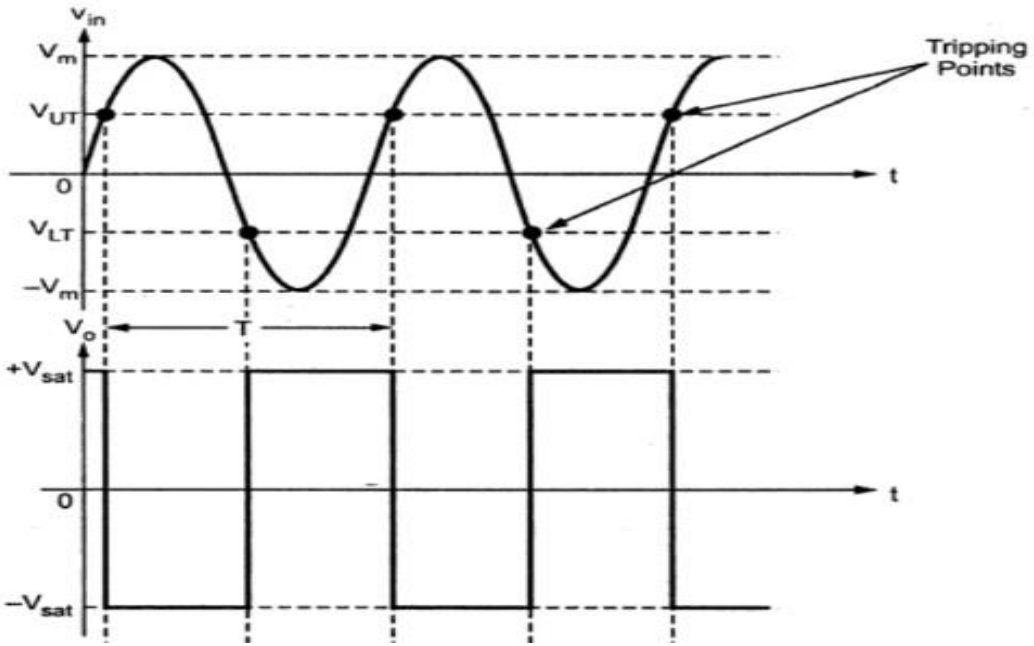
$$V_{UT} = V_{ref}\frac{R1}{R1+R2} + V_{sat}\frac{R2}{R1+R2}$$

As long as Vi is less than the Vut the output remains +Vsat .When ever the input voltage exceeds the Vut the output shifts to –Vsat and remains constant till the input voltage is greater than Vlt. When Vi become lesser than VLt then the output switches from –Vsat to +Vsat .

Schmitt trigger

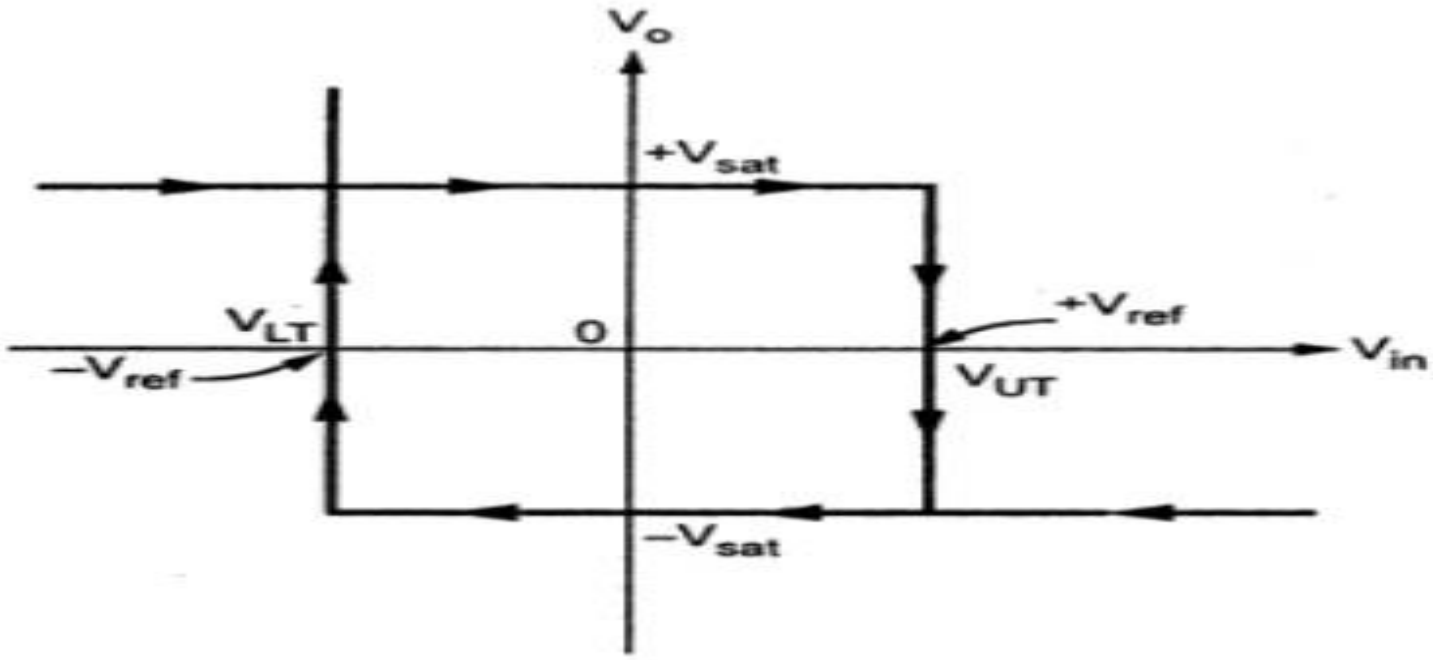
- Va =VLT (lower threshold voltage) for Vo=–Vsat then

$$V_{LT} = V_{ref}\frac{R1}{R1+R2} - V_{sat}\frac{R2}{R1+R2}$$



Vi < VLt ,Vo = +Vsat
Vi >Vut , Vo = -Vsat
VLt < Vut

Transfer Characteristic of Schmitt Trigger

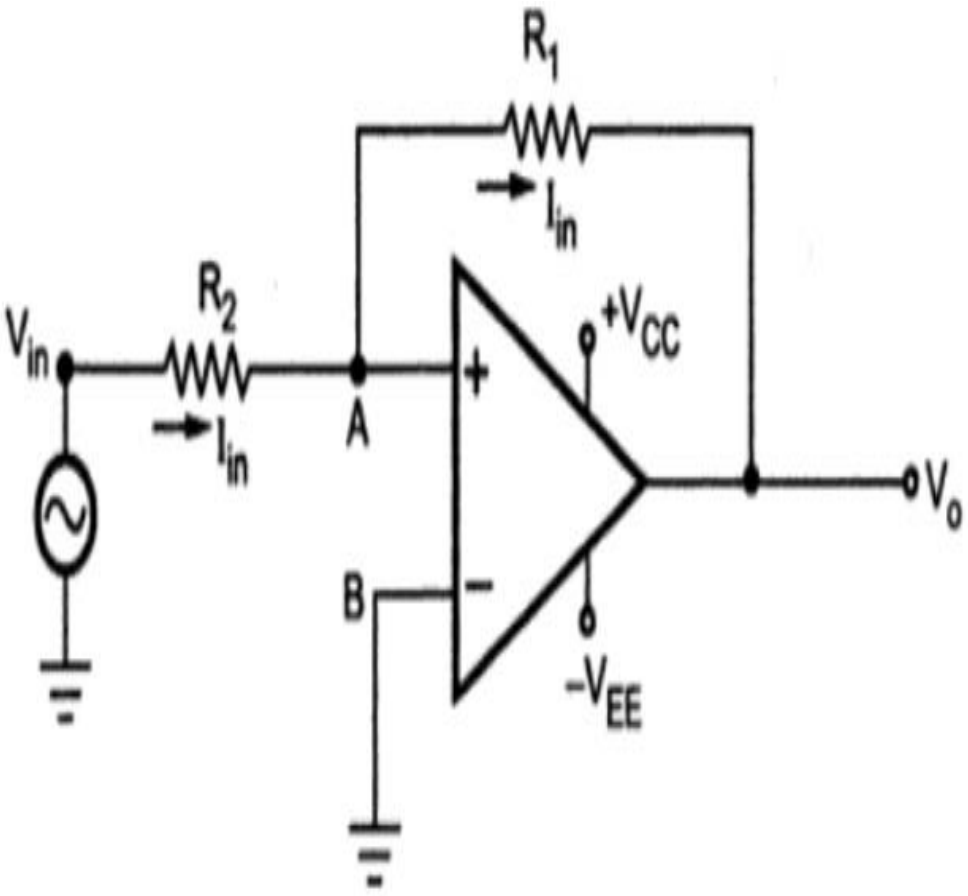


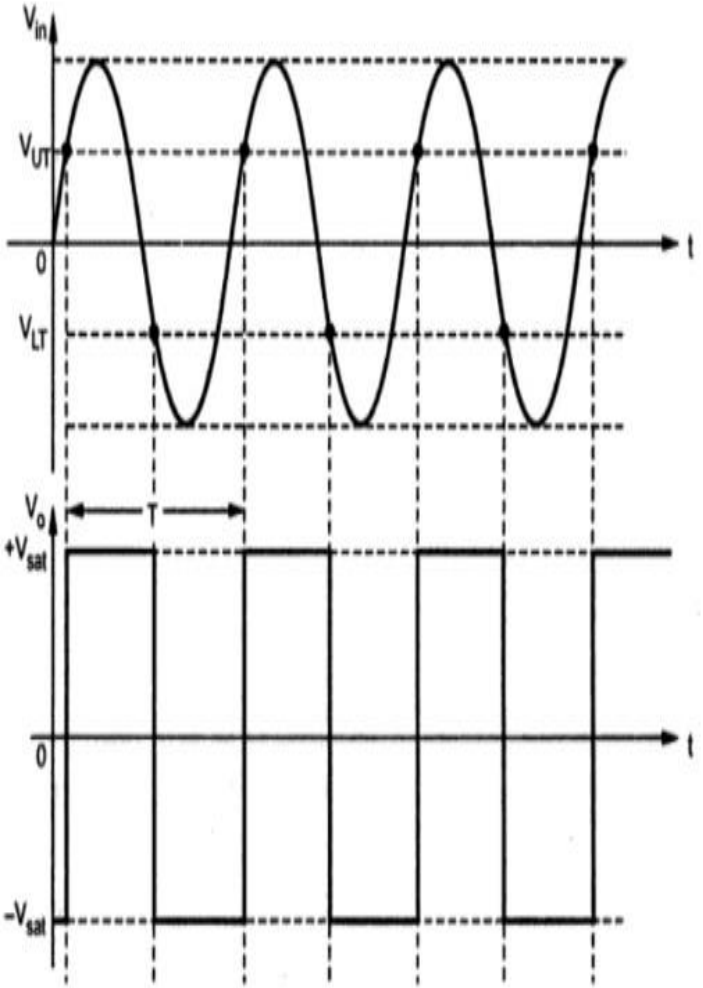
Schmitt trigger

- This circuit exhibits a interesting phenomenon called hysteresis or backlash ,as the curve looking like the hysteresis curve of magnetic materials . The difference between the two voltages(Vut,VLt) is called hysteresis voltage or hysteresis width. Because of hysteresis the circuit triggers at a higher voltage for increasing signals than for decreasing signals. if the peak-to-peak noise voltage is within the hysteresis voltage ,there will be no false triggering .Depending on the expected noise voltage ,the hysteresis voltage can be designed by the feedback resistors R1 and R2.

$$V_H = V_{UT} - V_{LT} = \frac{2R_2V_{sat}}{R_1 + R_2}$$

Non-Inverting Schmitt Trigger Circuit



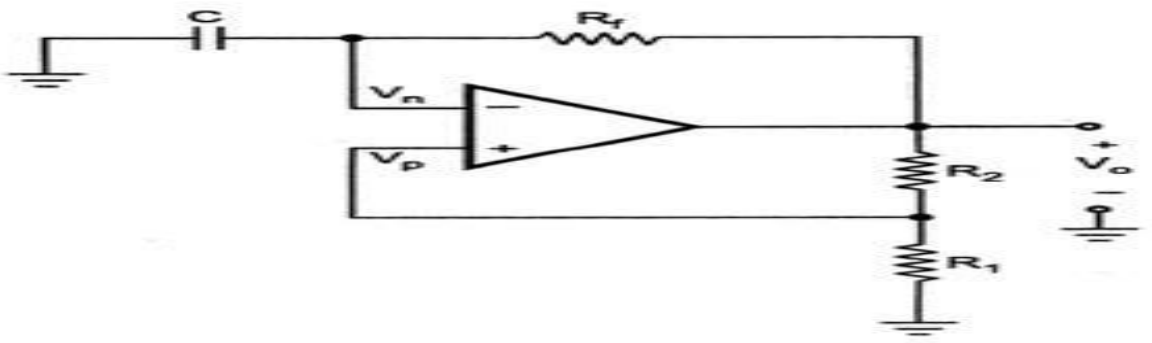


Astable Multivibrator

- The **astable multivibrator** is also called as **a free-running multivibrator.** It has **two** quasi-stable states i.e. no stable state such. **No external signal** is required to produce the changes in state. The component values used to decide the time for which circuit remains in each state. Usually, as the astable multivibrator oscillates between two states, is used to produce **a square wave.**

Astable Multivibrator

- The circuit looks like a Schmitt trigger except that the input voltage is replaced by a capacitor. As shown, the comparator and positive feedback resistors and form an inverting Schmitt trigger.



Circuit operation

(i). When power is turned ON, V_0 automatically swings either V_{sat} or to $-V_{sat}$ since these are the only stable states allowed by Schmitt trigger. Assume it swings to $+V_{sat}$.

(ii). Now capacitor starts charging towards $+V_{sat}$ through the feedback path provided by the resistor R_f to the inverting input. As long as the capacitor voltage V_C is less than V_{UT}, the output voltage remains at V_{sat}

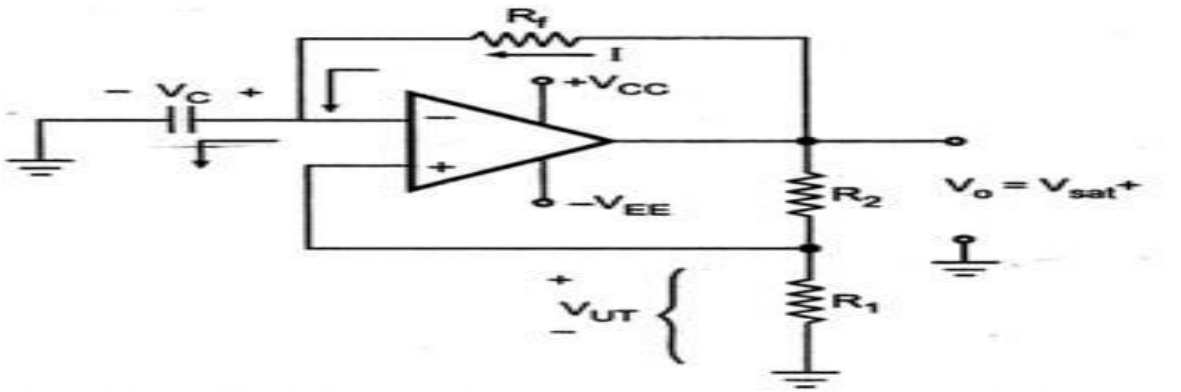


Fig. 6.16 (a) When $V_o = +V_{sat}$, capacitor charges towards V_{UT}

Circuit operation

(iii). As soon as V_C charges to a value slightly greater than V_{UT}, the input goes positive with respect to the input. This switches the output voltage from $+V_{sat}$ to $-V_{sat}$

(iv). As V_0 switches to $-V_{sat}$, capacitor starts discharging via . The current I discharges capacitor to 0 V and recharges capacitor to V_{LT} When V_C becomes slightly more negative than the feedback voltage V_{LT} output voltage switches back to $+V_{sat}$.

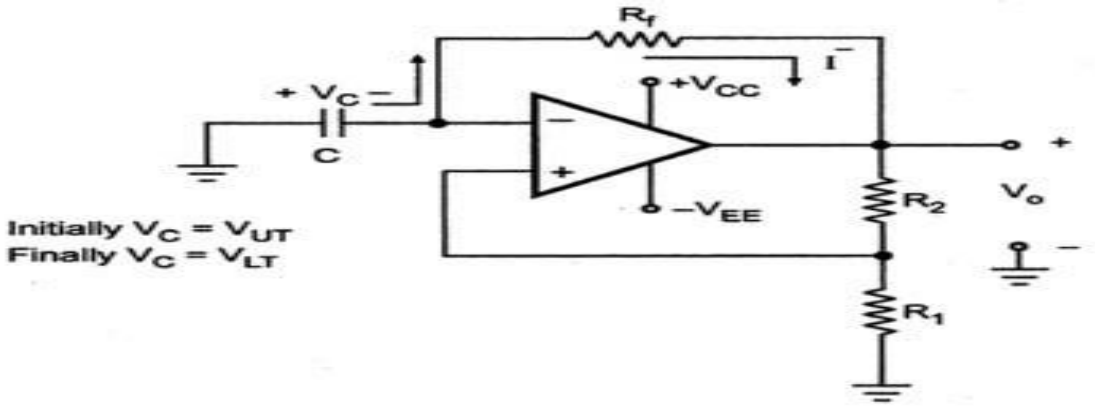
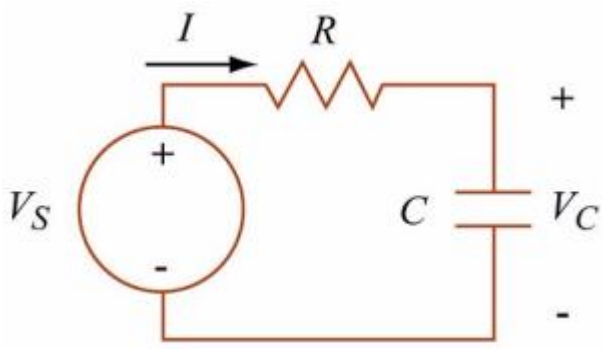


Fig. 6.16 (b) When $V_o = -V_{sat}$, capacitor charges towards V_{LT}

Frequency of Oscillation

- The frequency of oscillation is determined by the time it takes the capacitor to charge
- Initial voltage (at t=0) across Capacitor

$$\Rightarrow V_{C0} = -\beta V_{sat}$$



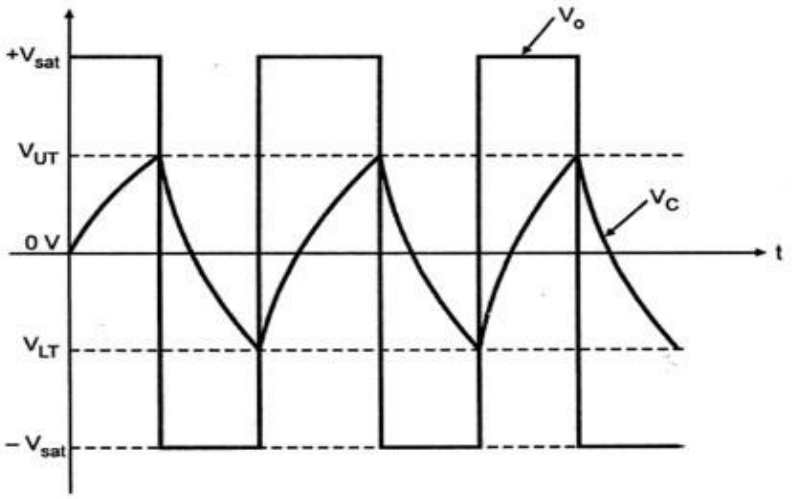


Fig. 6.16 (c) Waveforms

Frequency of Oscillation

Here Role of supply Voltage will play, the output voltage

$$V_s = V_0 = +V_{sat}$$

Voltage across Capacitor at time t is given by the eq

$$V_C(t) = V_{CO}e^{-\frac{t}{RC}} + V_0\left(1 - e^{-\frac{t}{RC}}\right)$$

At time $t = T_C$

$$V_0 = -V_{sat}$$

$$V_C(T_C) = +\beta V_{sat}$$

Frequency of Oscillation

$$V_C(t) = \left(V_{CO} - V_0\right) e^{-\frac{t}{RC}} + V_0$$

$$+\beta V_{sat} = \left(-\beta V_{sat} + V_{sat}\right) e^{-\frac{T_C}{RC}} + V_{sat}$$

$$T_C = RC \ \ln\left(\frac{1+\beta}{1-\beta}\right)$$

$$\beta = \frac{R_2}{R_1 + R_2}$$

$$T_C = T_d$$

Total time period (T)

$$T = T_C + T_d$$

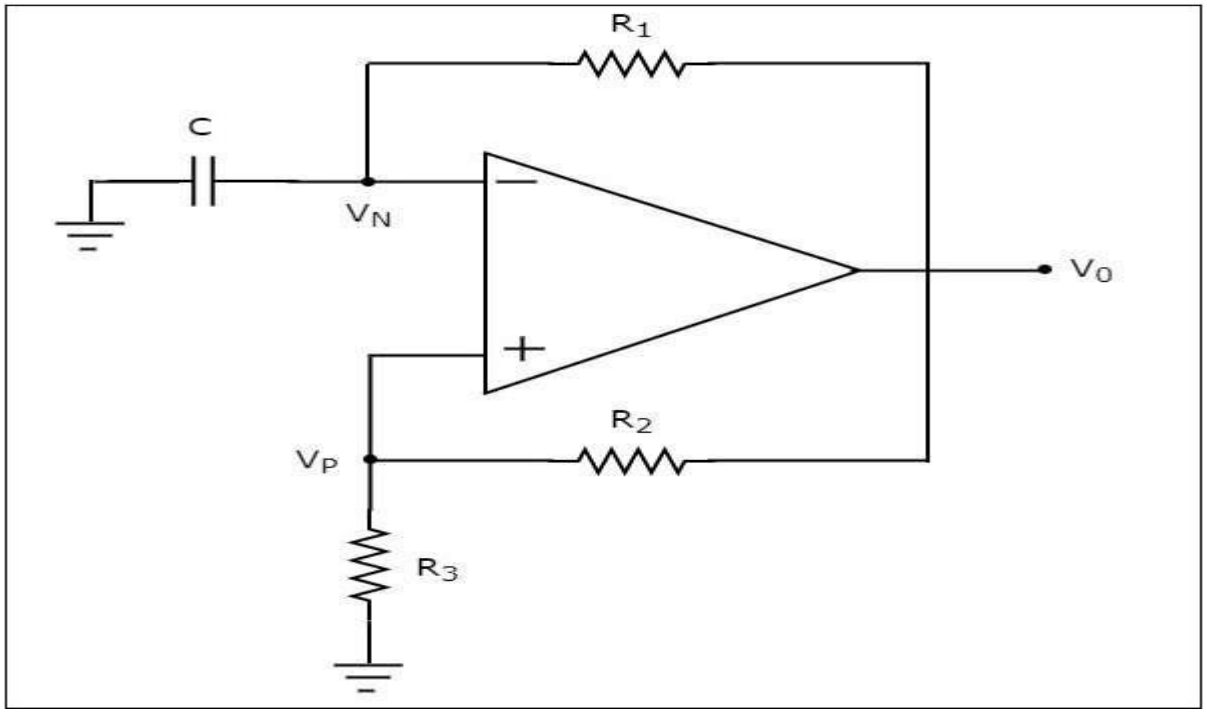
$$\boxed{T = 2RC \ \ln\left(\frac{1+\beta}{1-\beta}\right)}$$

Waveform Generators

- A **waveform generator** is an electronic circuit, which generates a standard wave. There are two types of op-amp based waveform generators −
- Square wave generator
- Triangular wave generator

Square Wave Generator

- A **square wave generator** is an electronic circuit which generates square wave



Square Wave Generator

- The resistor R1 is connected between the inverting input terminal of the op-amp and its output of op-amp. So, the resistor R1 is used in the **negative feedback**. Similarly, the resistor R2 is connected between the noninverting input terminal of the op-amp and its output. So, the resistor R2 is used in the **positive feedback** path.

Square Wave Generator

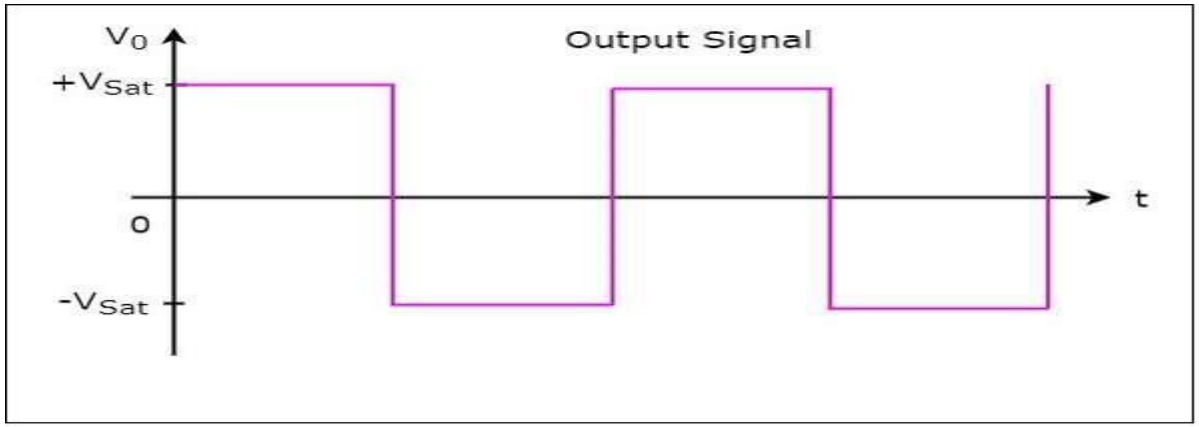
- A capacitor C is connected between the inverting input terminal of the op-amp and ground. So, the **voltage across capacitor C** will be the input voltage at this inverting terminal of op-amp. Similarly, a resistor R3 is connected between the non-inverting input terminal of the op-amp and ground. So, the **voltage across resistor** R3 will be the input voltage at this non-inverting terminal of the op-amp.

Square Wave Generator

- Assume, there is **no charge** stored in the capacitor initially. Then, the voltage present at the inverting terminal of the op-amp is zero volts. But, there is some offset voltage at non-inverting terminal of op-amp. Due to this, the value present at the output of above circuit will be +Vsat.
- Now, the capacitor C starts **charging** through a resistor R1. The value present at the output of the above circuit will change to −Vsat, when the voltage across the capacitor C reaches just greater than the voltage (positive value) across resistor R3.
- The capacitor C starts **discharging** through a resistor R1, when the output of above circuit is −Vsat. The value present at the output of above circuit will change to +Vsat,when the voltage across capacitor C reaches just less than (more negative) the voltage (negative value) across resistor R3

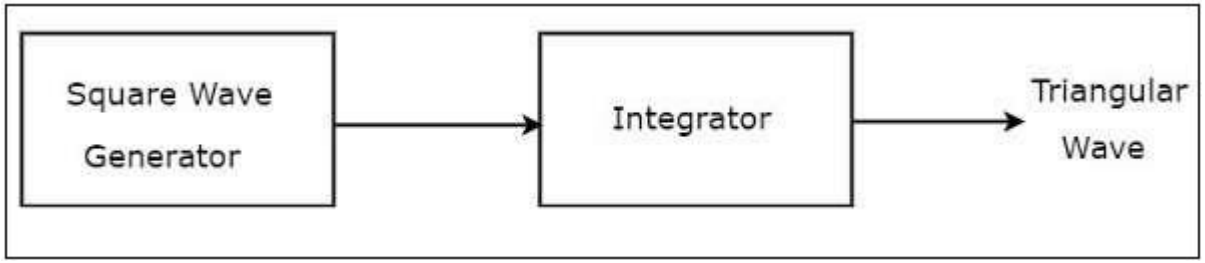
Square Wave Generator

The output of square wave generator will have one of the two values: +Vsat and −Vsat. So, the output remains at one value for some duration and then transitions to another value and remains there for some duration. In this way, it continues.



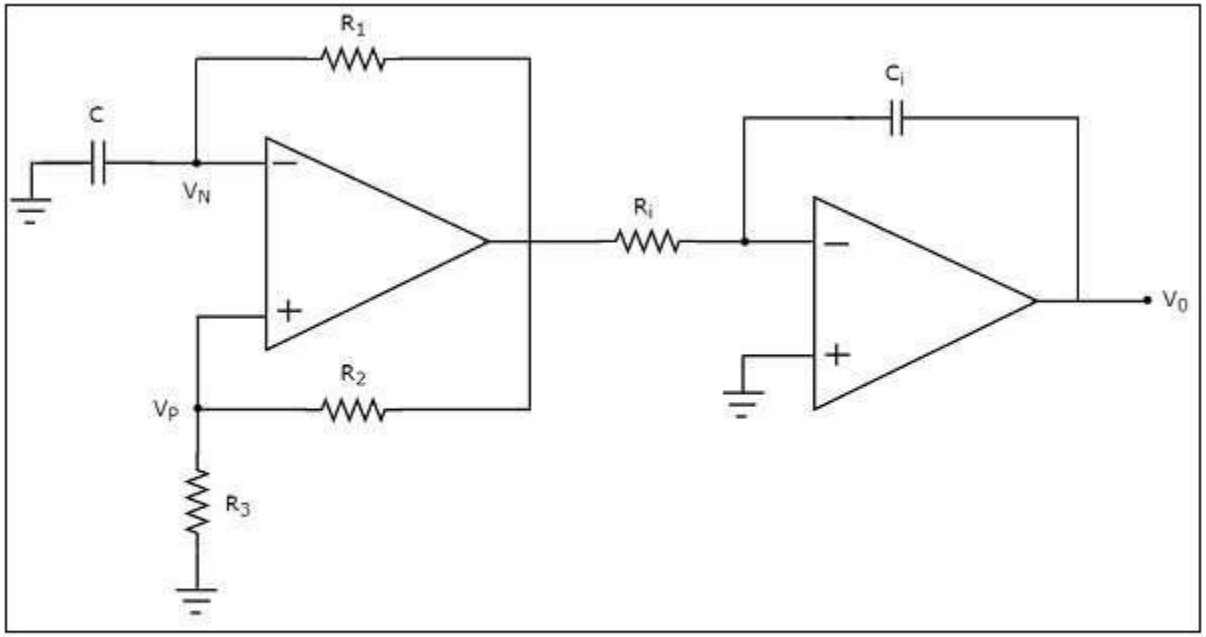
Triangular Wave Generator

- A triangular wave generator is an electronic circuit, which generates a triangular wave.



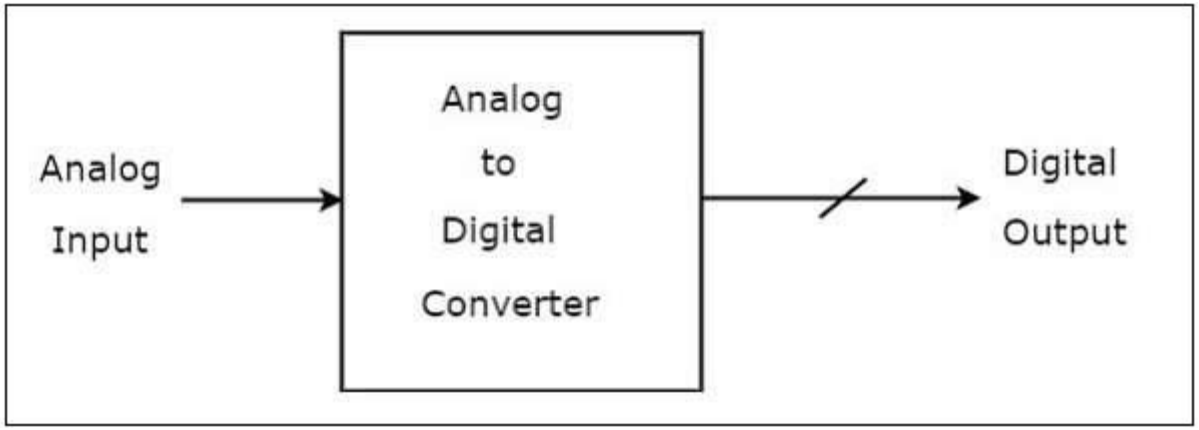
The block diagram of a triangular wave generator contains mainly two blocks: a square wave generator and an integrator. These two blocks are **cascaded**. That means, the output of square wave generator is applied as an input of integrator. Note that the integration of a square wave is nothing but a triangular wave.

Triangular Wave Generator



Analog to Digital Converter

- An Analog to Digital Converter **(ADC)** converts an analog signal into a digital signal. The digital signal is represented with a binary code, which is a combination of bits 0 and 1.



Analog to Digital Converter

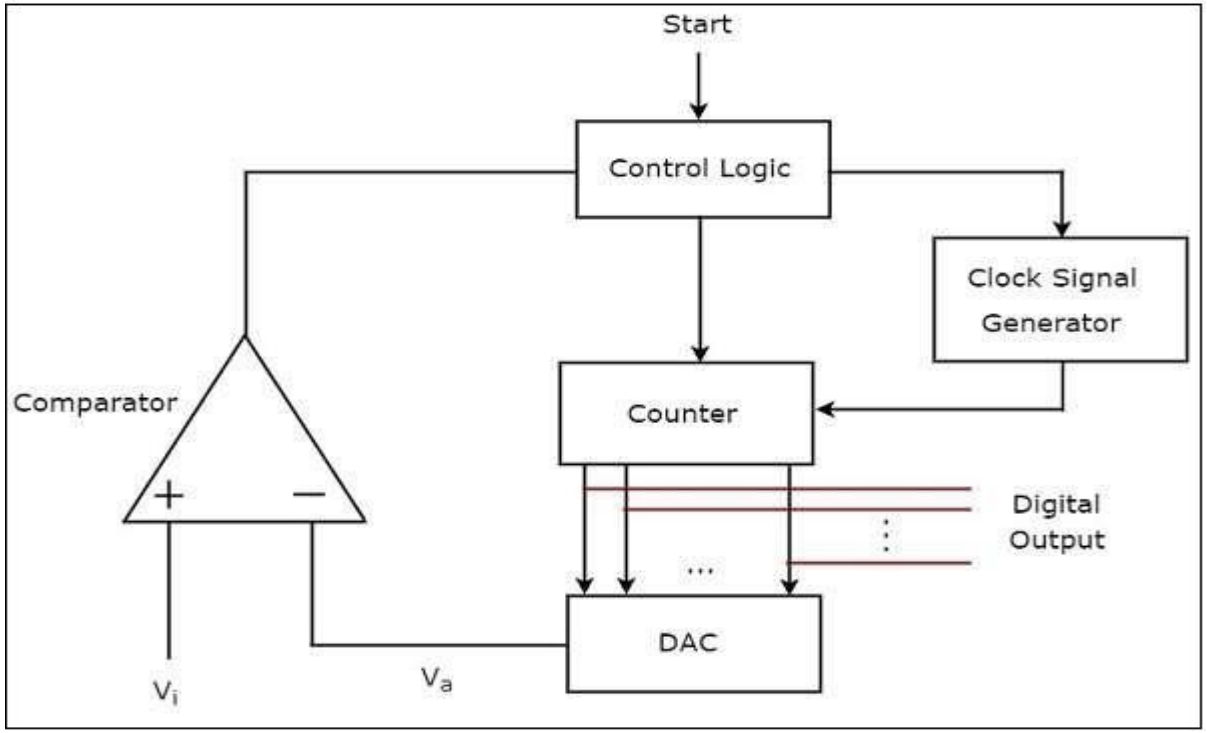
- Analog to Digital Converter **(ADC)** consists of a single analog input and many binary outputs. In general, the number of binary outputs of ADC will be a power of two.
- There are **two types** of ADCs: Direct type ADCs and Indirect type ADC.

Direct type ADC.

- The following are the **examples** of Direct type ADCs –
- Counter type ADC
- Successive Approximation ADC
- Flash type ADC

Counter type ADC

- A **counter type ADC** produces a digital output, which is approximately equal to the analog input by using counter operation internally.



Counter type ADC

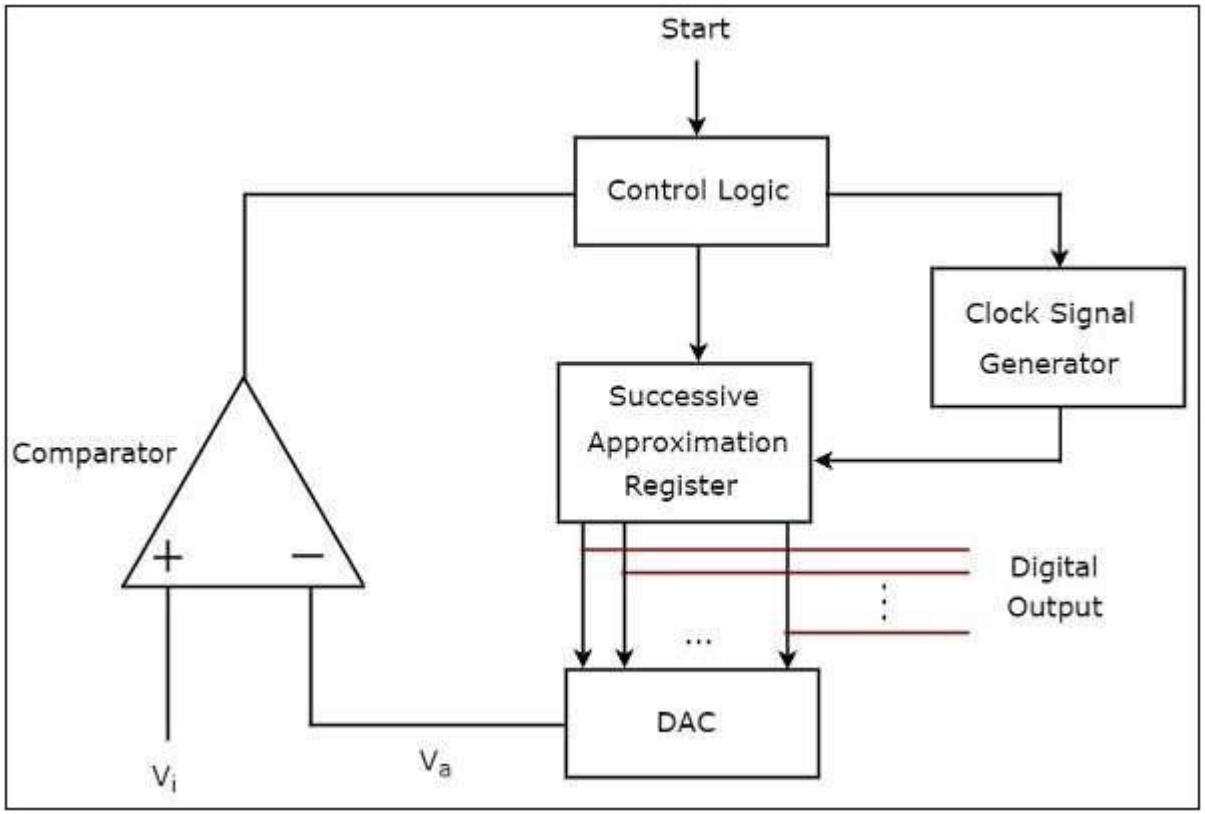
- The counter type ADC mainly consists of 5 blocks: Clock signal generator, Counter, DAC, Comparator and Control logic.
- The **working** of a counter type ADC is as follows −
- The **control logic** resets the counter and enables the clock signal generator in order to send the clock pulses to the counter, when it received the start commanding signal.
- The **counter** gets incremented by one for every clock pulse and its value will be in binary (digital) format. This output of the counter is applied as an input of DAC.
- **DAC** converts the received binary (digital) input, which is the output of counter, into an analog output. Comparator compares this analog value,Va with the external analog input value Vi.

Counter type ADC

- The **output of comparator** will be **‘1’** as long as Vi is greater than Va. The operations mentioned in above two steps will be continued as long as the control logic receives ‘1’ from the output of comparator.
- The **output of comparator** will be **‘0’** when Vi is less than or equal to Va. So, the control logic receives ‘0’ from the output of comparator. Then, the control logic disables the clock signal generator so that it doesn’t send any clock pulse to the counter.
- At this instant, the output of the counter will be displayed as the **digital output**. It is almost equivalent to the corresponding external analog input value Vi.

Successive Approximation ADC

- A **successive approximation type ADC** produces a digital output, which is approximately equal to the analog input by using successive approximation technique internally**.**



Successive Approximation ADC

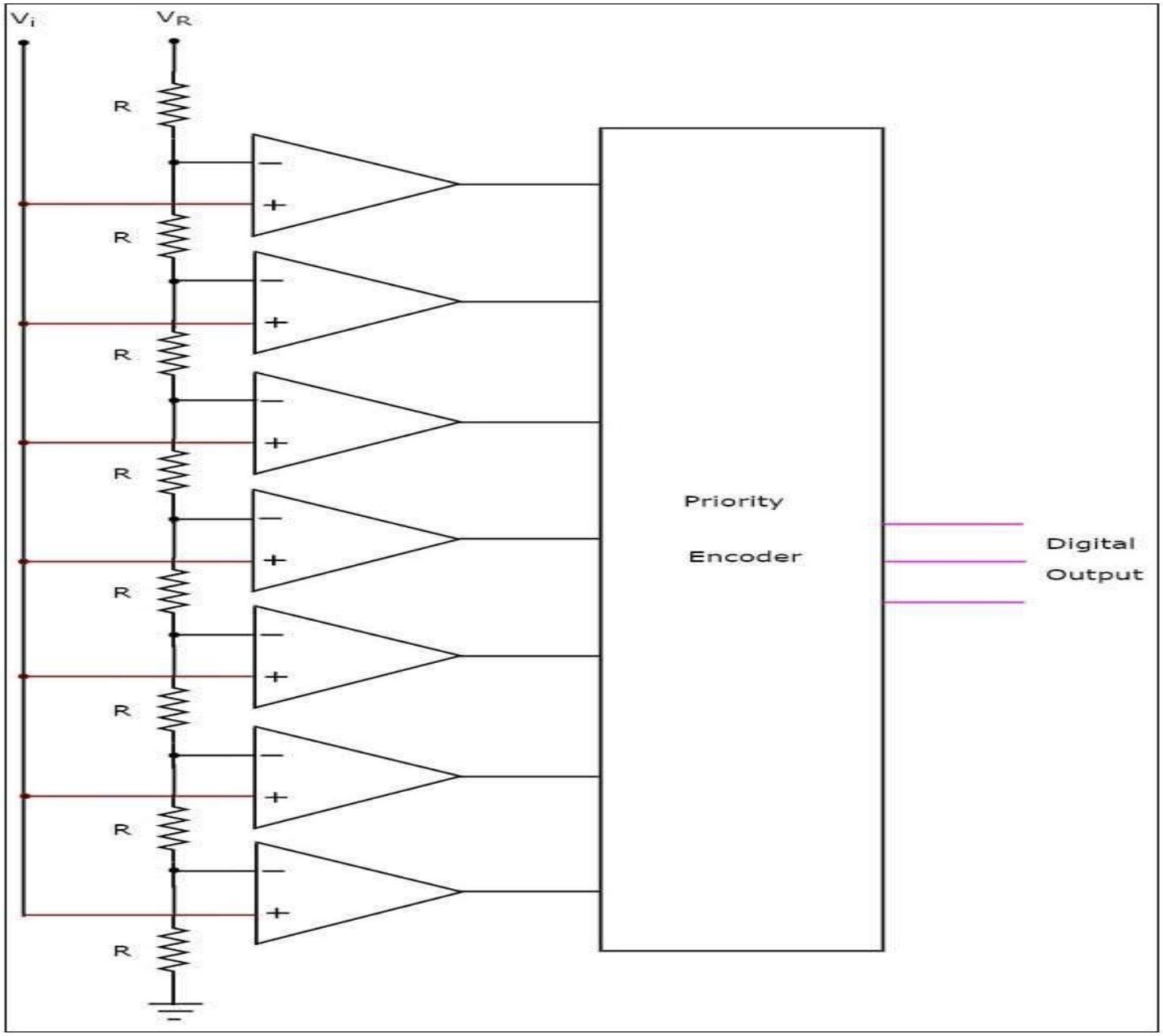
- The successive approximation ADC mainly consists of 5 blocks− Clock signal generator, Successive Approximation Register (SAR), DAC, comparator and Control logic.
- The **working** of a successive approximation ADC is as follows −
- The **control logic** resets all the bits of SAR and enables the clock signal generator in order to send the clock pulses to SAR, when it received the start commanding signal.
- The binary (digital) data present in **SAR** will be updated for every clock pulse based on the output of comparator. The output of SAR is applied as an input of DAC.

Successive Approximation ADC

- **DAC** converts the received digital input, which is the output of SAR, into an analog output. The comparator compares this analog value Va with the external analog input value Vi.
- The **output of a comparator** will be ‘1’ as long as Vi is greater than Va. Similarly, the output of comparator will be ‘0’, when Vi is less than or equal to Va.
- The operations mentioned in above steps will be continued until the digital output is a valid one.
- The digital output will be a valid one, when it is almost equivalent to the corresponding external analog input value Vi.

Flash type ADC

- A **flash type ADC** produces an equivalent digital output for a corresponding analog input in no time. Hence, flash type ADC is the fastest ADC.
- The 3-bit flash type ADC consists of a voltage divider network, 7 comparators and a priority encoder


Vi
VR
R
R
R
R
R
R
R
R
Priority
Encoder
Digital
Output

.

The **working** of a 3-bit flash type ADC is as follows.

•The **voltage divider network** contains 8 equal resistors. A reference voltage VR is applied across that entire network with respect to the ground. The voltage drop across each resistor from bottom to top with respect to ground will be the integer multiples (from 1 to 8) of VR8.

•The external **input voltage** Vi is applied to the non-inverting terminal of all comparators. The voltage drop across each resistor from bottom to top with respect to ground is applied to the inverting terminal of comparators from bottom to top.

•At a time, all the comparators compare the external input voltage with the voltage drops present at the respective other input terminal. That means, the comparison operations take place by each comparator **parallel**.

Flash type ADC

•The **output of the comparator** will be ‘1’ as long as Vi is greater than the voltage drop present at the respective other input terminal. Similarly, the output of comparator will be ‘0’, when, Vi is less than or equal to the voltage drop present at the respective other input terminal.
•All the outputs of comparators are connected as the inputs of **priority encoder**.This priority encoder produces a binary code (digital output), which is corresponding to the high priority input that has ‘1’.
•Therefore, the output of priority encoder is nothing but the binary equivalent **(digital output)** of external analog input voltage, Vi
The flash type ADC is used in the applications where the conversion speed of analog input into digital data should be very high.

Indirect Type ADC

- If an ADC performs the analog to digital conversion by an indirect method, then it is called an **Indirect type ADC**. In general, first it converts the analog input into a linear function of time (or frequency) and then it will produce the digital (binary) output.

Dual Slope ADC

- As the name suggests, a **dual slope ADC** produces an equivalent digital output for a corresponding analog input by using two (d
- The dual slope ADC mainly consists of 5 blocks: Integrator, Comparator, Clock signal generator, Control logic and Counter.ual) slope technique.

Dual Slope ADC

- The **control logic** resets the counter and enables the clock signal generator in order to send the clock pulses to the counter, when it is received the start commanding signal.
- Control logic pushes the switch **sw** to connect to the **external analog input voltage** ViVi, when it is received the start commanding signal. This input voltage is applied to an integrator.
- The output of the **integrator** is connected to one of the two inputs of the comparator and the other input of comparator is connected to ground.
- **Comparator** compares the output of the integrator with zero volts (ground) and produces an output, which is applied to the control logic.
- The **counter** gets incremented by one for every clock pulse and its value will be in binary (digital) format. It produces an overflow signal to the control logic, when it is incremented after reaching the maximum count value. At this instant, all the bits of counter will be having zeros only.

Dual Slope ADC

- Now, the control logic pushes the switch **sw** to connect to the **negative reference** voltage −Vref. This negative reference voltage is applied to an integrator. It removes the charge stored in the capacitor until it becomes zero.
- At this instant, both the inputs of a comparator are having zero volts. So, comparator sends a signal to the control logic. Now, the control logic disables the clock signal generator and retains (holds) the counter value.
  The **counter value** is proportional to the external analog input voltage.
- At this instant, the output of the counter will be displayed as the **digital output**. It is almost equivalent to the corresponding external analog input value Vi.

POST TEST:

1. An ideal Si diode is used in a half wave rectifier circuit with peak input sinusoidal signal amplitude of 5V (Vm = 5V & VT = 0.7V). The average dc voltage is

a)<1.27V

b)=1.37V

c)>1.87V

d) <2.54

2. Four ideal Si diodes [VT = 0.7V] are used in a bridge rectifier circuit which has a peak input sinusoidal signal amplitude of 5V [Vm = 5V]. The average DC voltage is
   a) <2.54

   b)=2.74

   c)>3.74

   d)=1.37V

3. For silicon diode with I_0 =2.5μA at 300K, find the forward voltage at a forward current of 10mA

   a) 0
   b) 5 V
   c) 4.3 V
   d) 0.4V

4. If peak voltage on a half wave rectifier circuit is 5V and diode cut-in voltage is 0.7, then peak inverse voltage on diode will be _____
   a) 3.6V
   b) 4.3V
   c) 5V
   d) 5.7V

5. For a diode, at 10mA DC resistance is 70Ω. The voltage corresponding to 10mA will be _____
   a) 0.5V
   b) 0.6V
   c) 0.7V
   d) 0.8V

6. A transistor has an I_C of 100mA and I_B of 0.5mA. What is the value of αdc?
   a) 0.787
   b) 0.995
   c) 0.543
   d) 0.659

7. In an NPN silicon transistor, α=0.995, I_E=10mA and leakage current I_{CBO}=0.5µA. Determine I_{CEO}.

a) 10µA

b) 100µA

c) 90µA

d) 500µA

8. If g_m=0.5mS, R_S=2KΩ, determine Z_O for source follower?

a) 2KΩ

b) 1KΩ

c) 3KΩ

d) 1.5KΩ

9. The current flowing into one input of the op-amp is 10nA and it is 14 nA in the other. Find the input offset current.

a) 1nA

b) -4nA

c) 4nA

d) 11nA

10. Calculate the cutoff frequency of a first-order low-pass filter for R1 =2.5kΩ and C1 = 0.05µF

a)1.273kHz

b)12.73kHz

c)127.3 kHz

d)127.3 Hz

ASSIGNMENT:

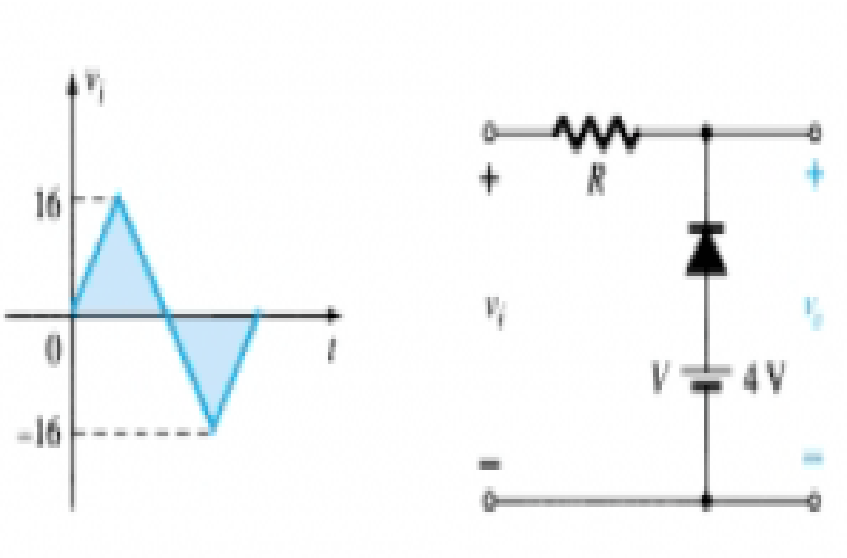
1. For the given input waveform to the given circuit, what is the minimum value of the output waveform?

a) 4 V

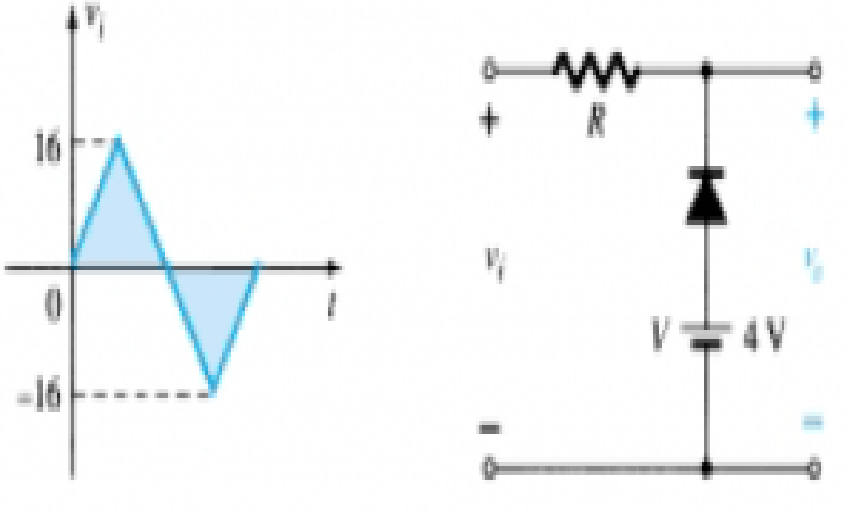
b) 16 V

c) 12 V

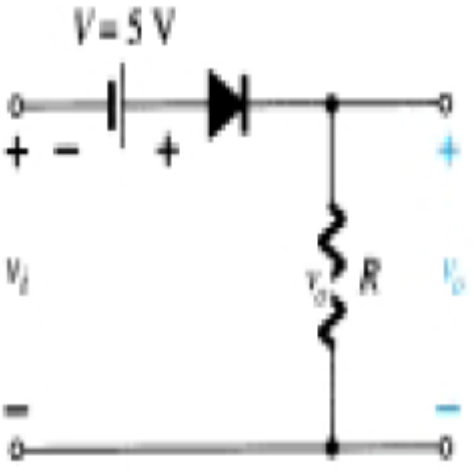
d) 0 V



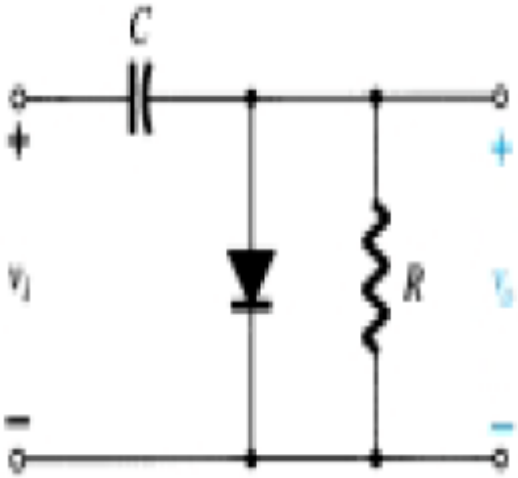
2. For the given input waveform to the given circuit, what is the peak value of the output waveform?
   a) 0 V
   b) 16 V
   c) 12 V
   d) 0 V



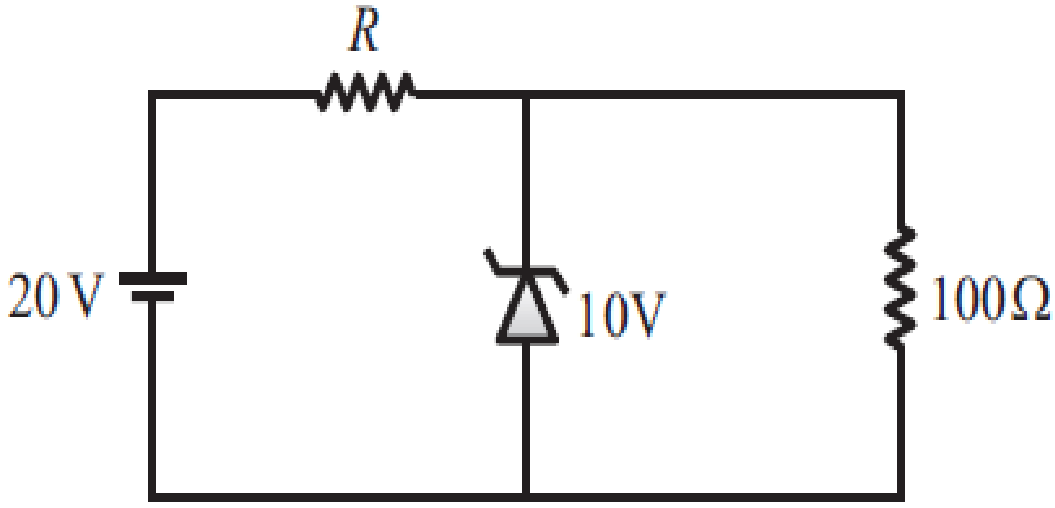
3. What is the circuit in the given diagram called?
   a) Clipper
   b) Clamper
   c) Half wave rectifier
   d) Full wave rectifier



4. What is the circuit in the given diagram called?
   a) Clipper
   b) Clamper
   c) Half wave rectifier
   d) Full wave rectifier

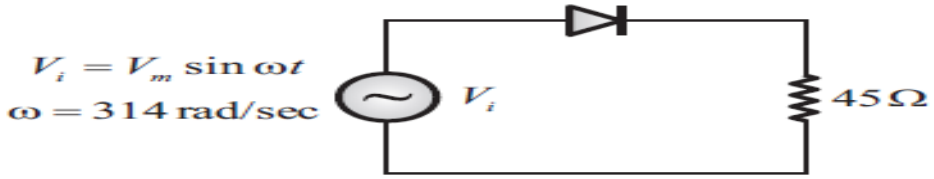


5. Figure shows an electronic voltage regulator. The Zener diode may be assumed to require a minimum current of 25 mA for satisfactory operations. The value of *R (in ohms) required for* satisfactory voltage regulation of the circuit is _____.



6.

The forward resistance of the diode shown in figure is 5 Ω and the remaining parameters are same as those of ideal diode. The DC components of the source current is



(A) $\frac{V_m}{50\ \pi}$

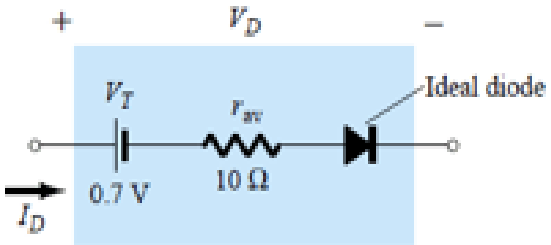
(B) $\frac{V_m}{50\ \pi\sqrt{2}}$

(C) $\frac{V_m}{100\ \pi\sqrt{2}}$

(D) $\frac{2V_m}{50\ \pi\sqrt{2}}$

7. Which model of the diode equivalent circuit is represented by the given diagram?

a) Piecewise Linear Model
b) Ideal Diode Model
c) Simplified Model
d) Differential Model



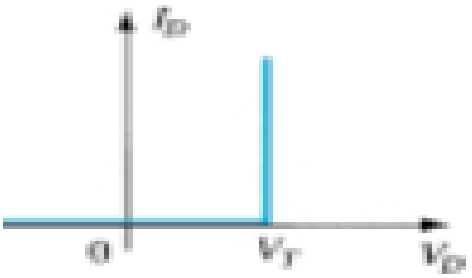
8. Which of the following models of diode equivalent circuit is represented by the given I-V characteristic curve?

a) Piecewise Linear Model

b) Ideal Diode Model

c) Simplified Model

d) Hybrid model



9. As temperature is increased, the voltage across a diode carrying a constant current.

a) Increases

b)Decrease

c)Remains Constant

d)May increase or decrease depending upon the doping levels in the junctions

10. For small signal ac operation, a practical forward biased diode can be modeled as

a) Resistance and capacitance in series

b) Ideal diode and resistance in parallel

c) Resistance and ideal diode in series

d) Resistance

11. In CE configuration, if the voltage drop across 5kΩ resistor connected in the collector circuit is 5V. Find the value of I_B when β=50.

a) 0.01mA

b) 0.25mA

c) 0.03mA

d) 0.02mA

12. For a Class B amplifier, the utilized load power is 300W and the Dc power is 500W, find efficiency.

a) 30%

b) 60%

c) 90%

d) 100%

13. A Self bias configuration contains R_D=3.3, R_s=1 KΩ, R_G=1MΩ and g_m=1.5mS. Determine A_v?

a) -2

b) 3

c) -4

d) 5

14. Find the input bias current if IB1 = 5mA ,IB2 =3mA

a) 8mA
b) 2mA
c) 4mA
d) None of the mentioned

15. Determine the period of oscillation for an astable multivibrator with component values RC = 20×10^{-3} and feedback factor = 0.3.

a) 0.55s
b) 0.9 s

c) 0.024 s

d) 0.7s

CONCLUSION:

1. Able to analyse and model diode based circuits.
2. Able to Design and analyze various rectifier, clipper and clamper circuits.
3. Able to Design and analyze various Amplifiers, Oscillators, Filters , Multivibrators circuits.

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